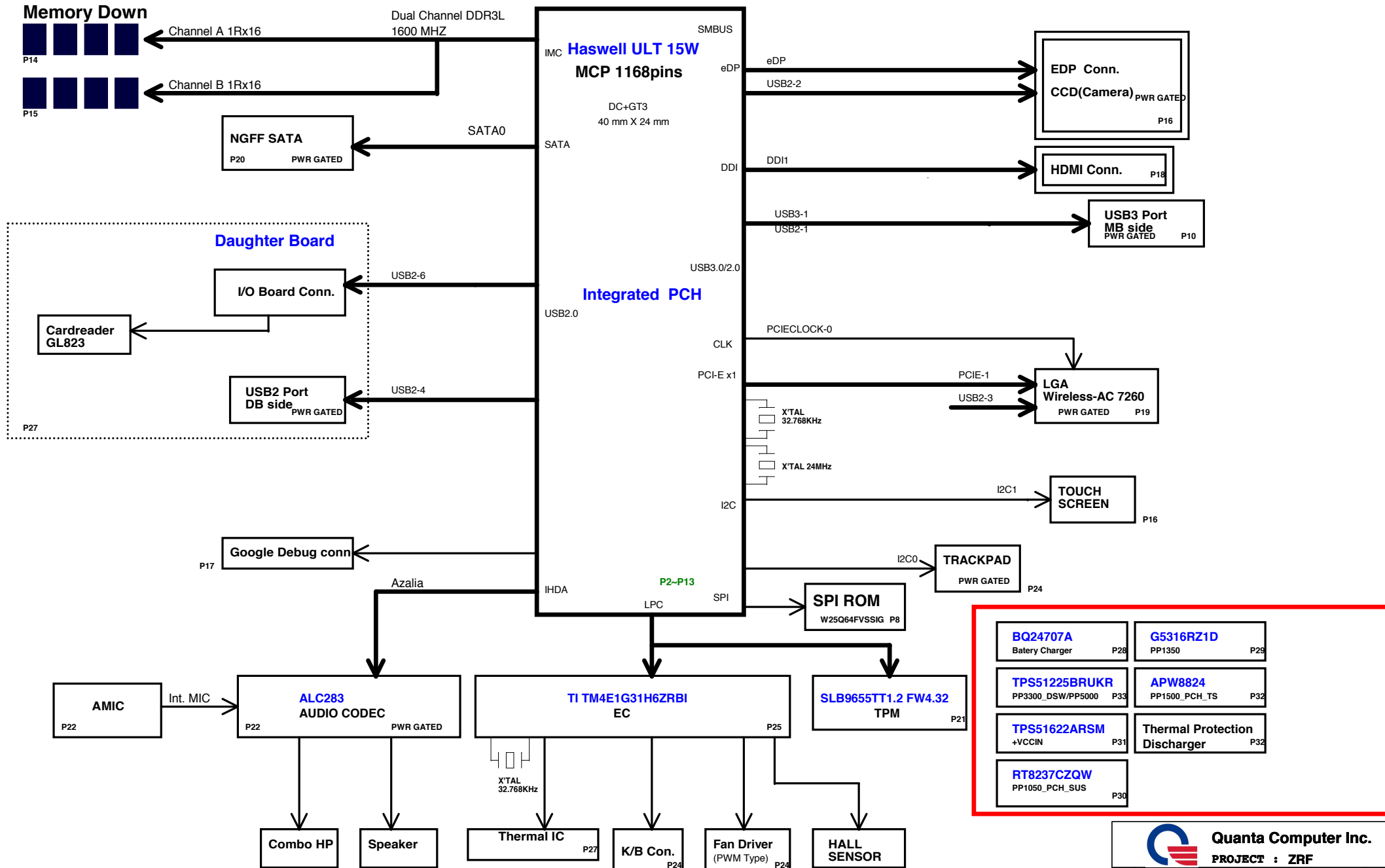


# Melvita (ZRF) SHB ULT SYSTEM BLOCK DIAGRAM

01

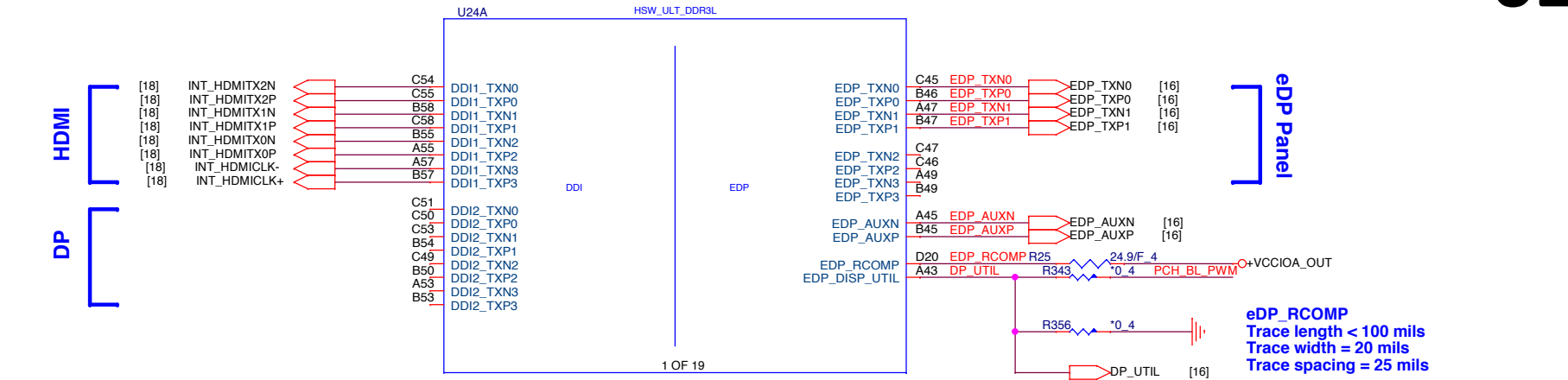


# Haswell ULT (DISPLAY,eDP)

02

HDMI  
DP

eDP Panel



Haswell C-1 2c BGA 1.6GHz ULV 15W 2+2 i5-4200U QS for proto/AJ0QEVEVT01

DDPB/C\_CTRLDATA has an iPD 20K.  
When PU at rising edge of PCH\_PWROK, the DDI port will be detected



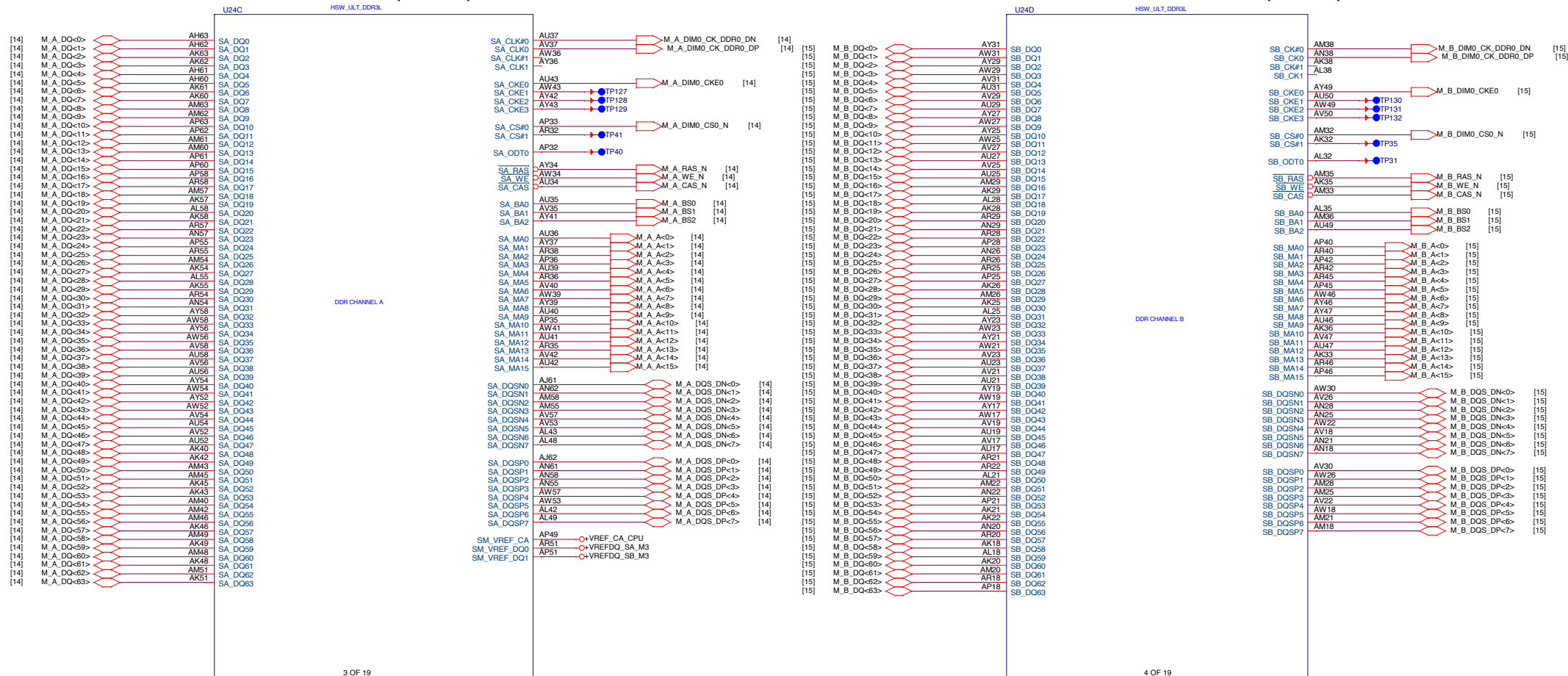
Quanta Computer Inc.

PROJECT : ZRF

Size	Document Number	Rev A
	Haswell 1/5 (DDI/eDP)	
Date:	Monday, January 12, 2015	Sheet 2 of 38

## Haswell ULT (DDR3L)

## Haswell Processor (DDR3L)



# Haswell ULT (SIDE BAND)

**H\_PECI (50ohm)**  
Route on microstrip only  
Spacing >18 mils  
Trace Length: 0.4~6.125 inches

**H\_PWRGOOD (50ohm)**  
Trace Length: 1~11.25 inches

**CPU\_PLTRST# (50ohm)**  
Trace Length: 10~17 inches

[25] H\_PECI

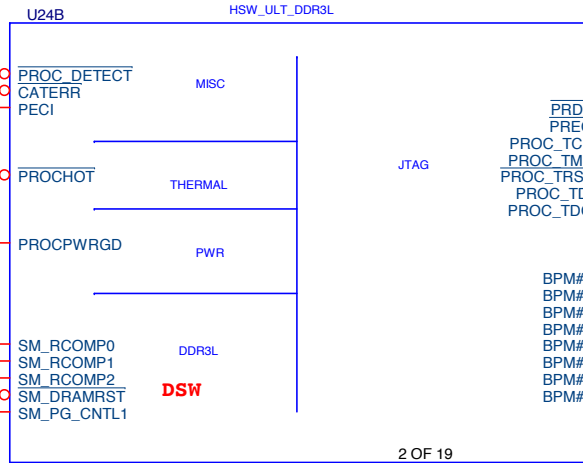
[17,25,28,31] H\_PROCHOT#

[25] CPU\_PGOOD

**SM\_RCOMP[0:2]**  
Trace length < 500 mils  
Trace width = 12~15 mils  
Trace spacing = 20 mils

SM\_RCOMP\_0 AU60  
SM\_RCOMP\_1 AV60  
SM\_RCOMP\_2 AU61  
CPU\_DRAMRST# AV15  
DDR\_PG\_CTRL AV61

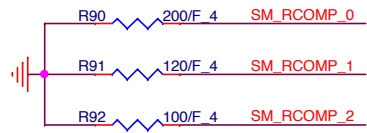
TP108



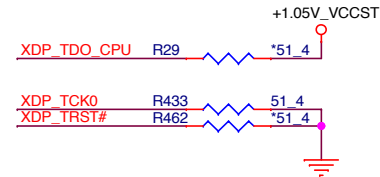
**TCK,TMS**  
Trace Length < 9000mils

**BPM#[0:7]**  
Trace Length 1~6 inches  
Length match < 300 mils

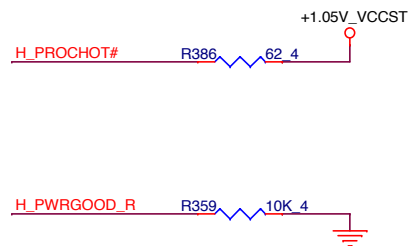
## DRAM COMP



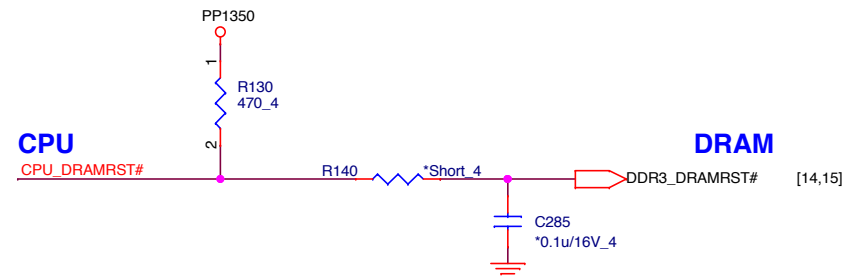
## XDP PU/PD



## PU/PD of CPU

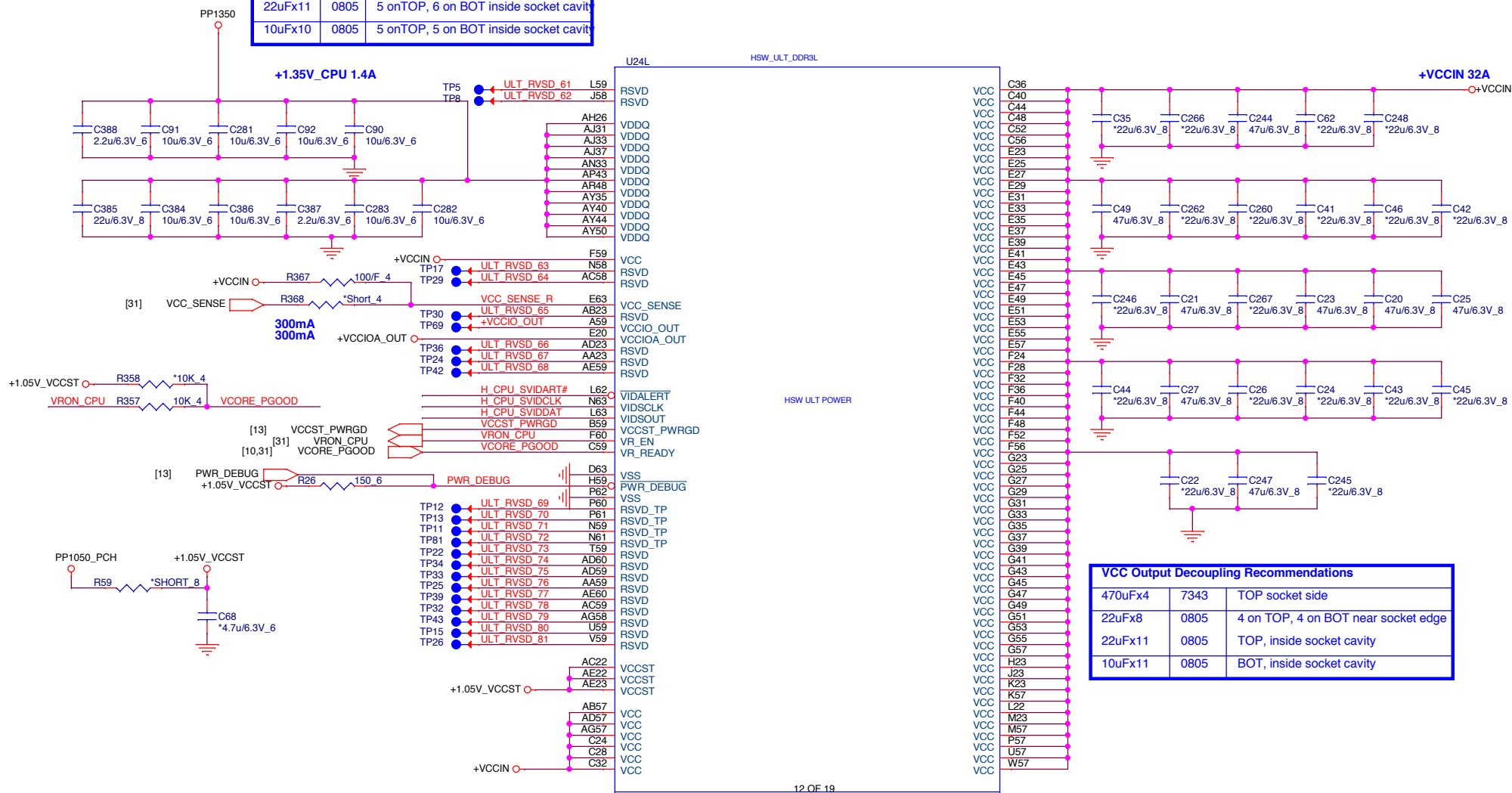


## DRAMRST

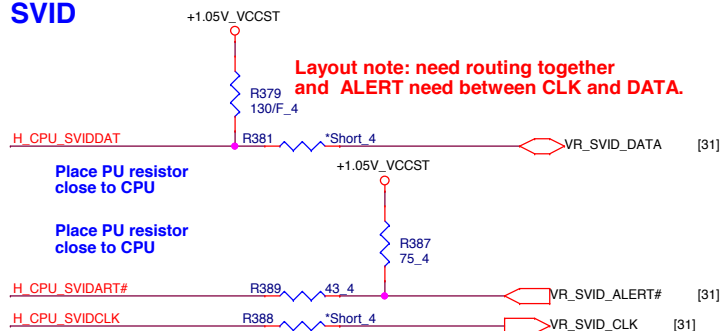


## Haswell ULT (POWER)

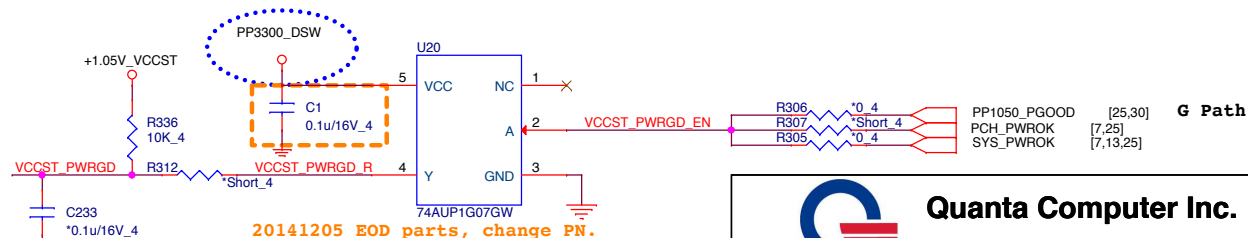
VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity



## SVID



**VCCST PWRGD**

**Quanta Computer Inc.**

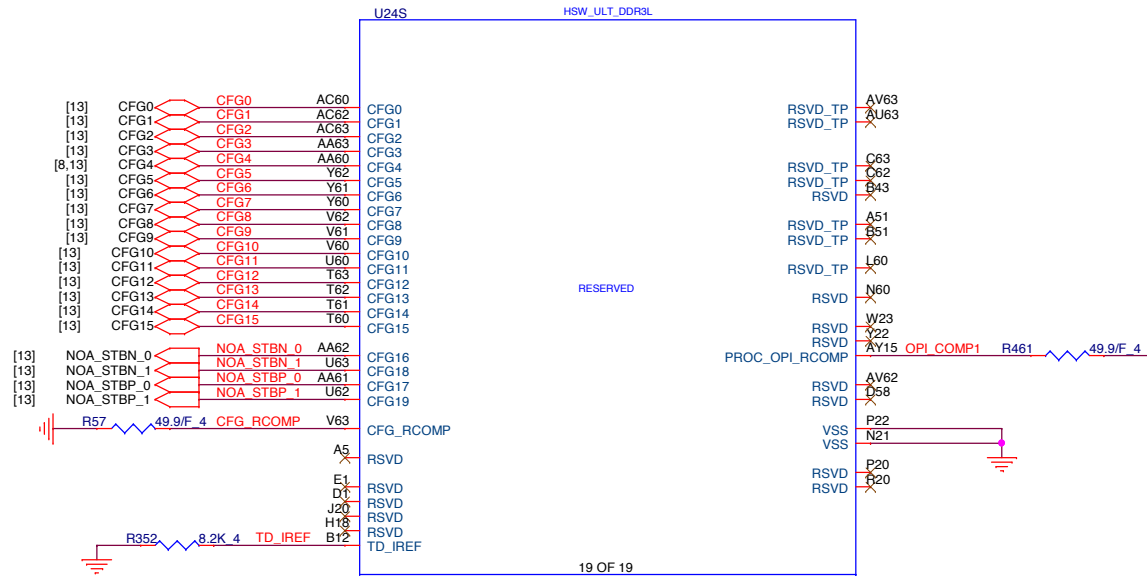
**PROJECT : ZRF**

**Haswell 4/5 (POWER)**

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# Haswell ULT (CFG,RSVD)

06



19 OF 19

## Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R417 *1K 4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R423 *1K 4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R409 *1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R403 *1K 4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R394 *1K 4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R56 *1K 4



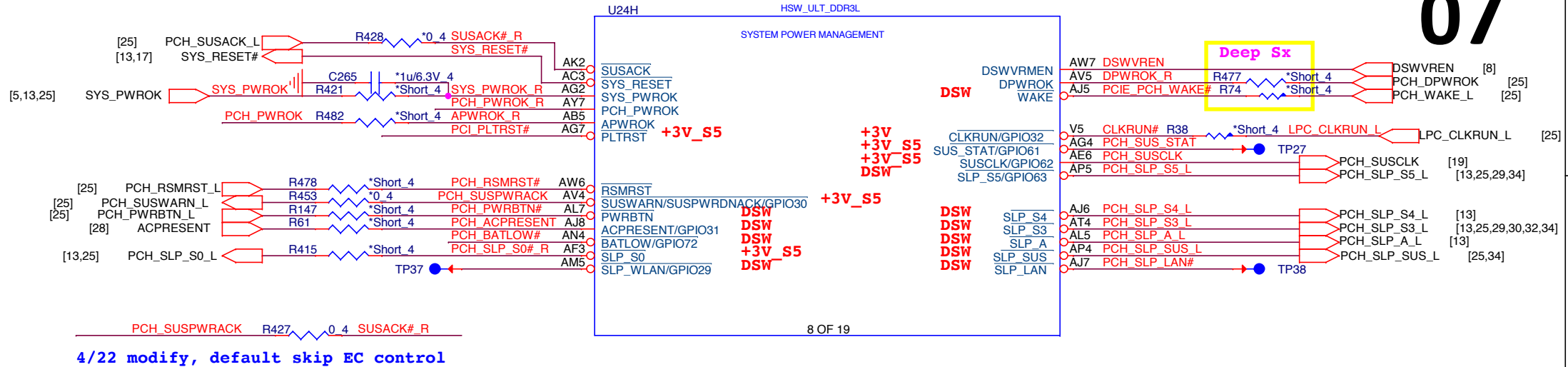
Quanta Computer Inc.

PROJECT : ZRF

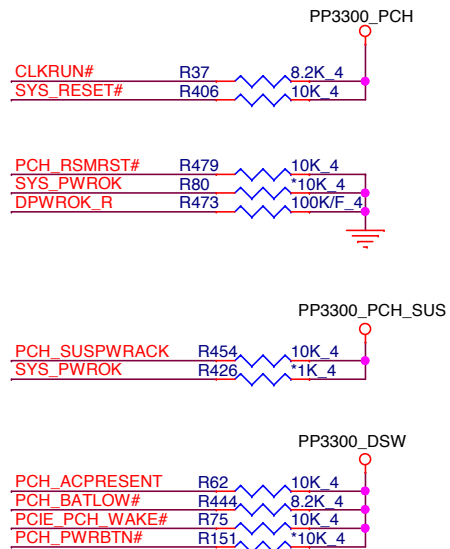
Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	A
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# Haswell ULT PCH (PM)

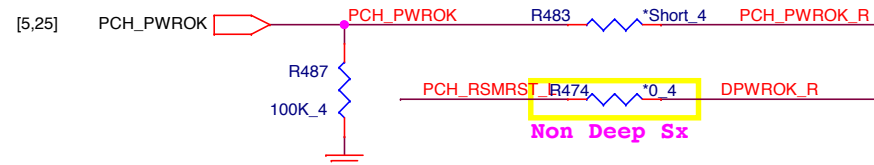
07



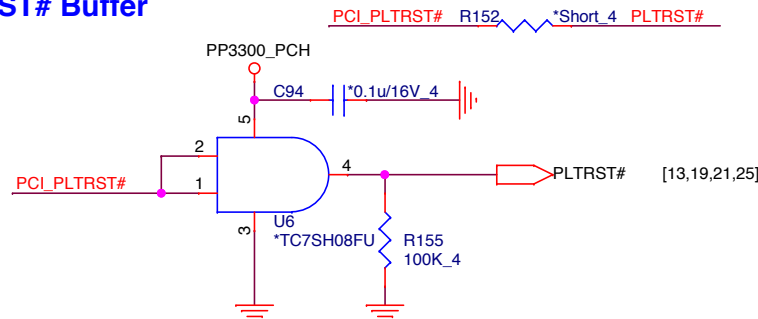
## PCH PM PU/PD



## PCH PWROK



## PLTRST# Buffer



4/22 modify, default is bypass PLTRST#



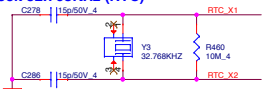
Quanta Computer Inc.

PROJECT : ZRF

Size	Document Number	Rev
	PCH 1/6 (PM)	A

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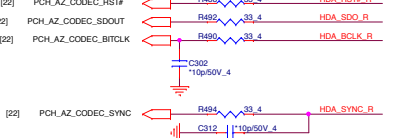
## RTC Clock 32.768KHz (RTC)



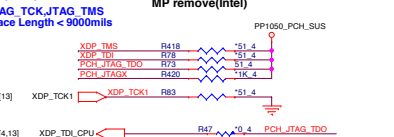
## RTC Circuitry (RTC)

+3V\_RTC  
Trace width = 30 mils+3V\_RTC  
Trace width = 20 mils  
20MIL

## HDA



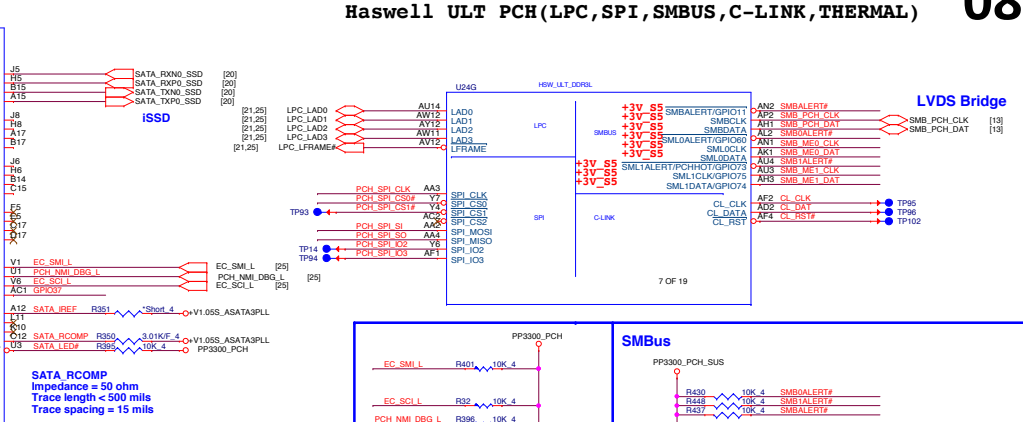
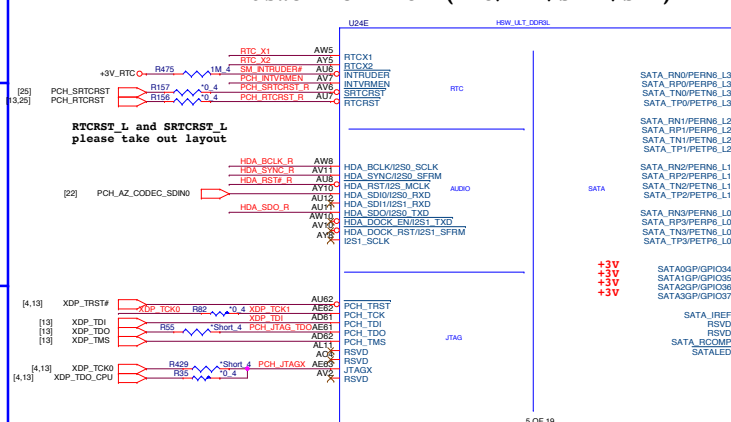
## PCH JTAG



## ULT Strapping Table

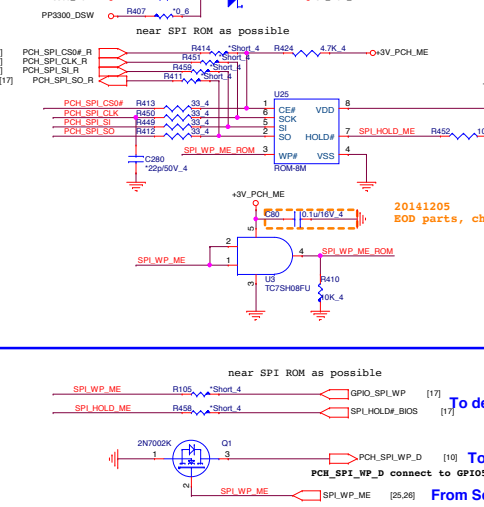
Pin Name	Strap description	Sampled	Configuration	Note
GPIO81 (SPKR)	No reboot on TCO Timer expiration	PWR0K	0 = Default enable (IPD 20K) 1 = Disable No-Reboot mode	PP3300_PCH R400 *1K 4 SPKR [10,22]
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWR0K	0 = Default can program ME (IPD 20K) 1 = can't program ME	HDA_SDO_R R493 *0.4 PCH HDA_SDO [9]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1 = Should be always pull-up	+3V_RTC R484 *330K 4 PCH INTRVDMEN R495 *330K 4
GPIO66	Top-Block Swap override		0 = Default disable (IPD 30K) 1 = Enable TBS function	PP3300_PCH R330 *1K 4 GPIO66 R340 *1K 4
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (IPD 20K) 1 = LPC	PP3300_PCH R1 *1K 4 GPIO86 R7 *1K 4
GPIO15	TLS (Transport layer security)		0 = Default enable w/o confidentiality (IPD 20K) 1 = Default enable with confidentiality	PP3300_PCH_SUS R50 *8.2K 4 GPIO15 R58 *1K 4
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 = disable	[6,13] CFG4 R64 *1K 4
DSWVREN	Deep Sx well on the VR enable		1 = Should be always pull-up	[7] DSWVREN R476 *330K 4 DSWVREN R472 *330K 4

## Haswell ULT PCH (RTC/HDA/SATA/SPI)

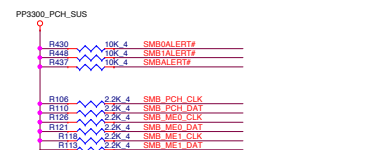


## PCH dual I/O SPI ROM

W25Q64FVSSIG(SOIC) / AKE3EPF0N06-----&gt;8MB

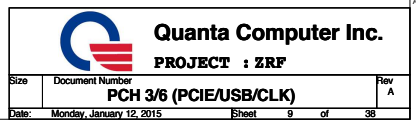


## SMBus

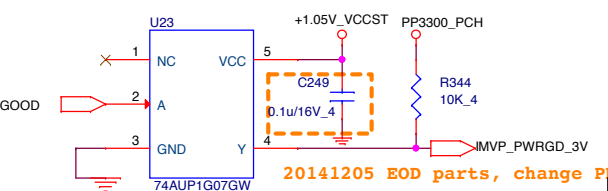
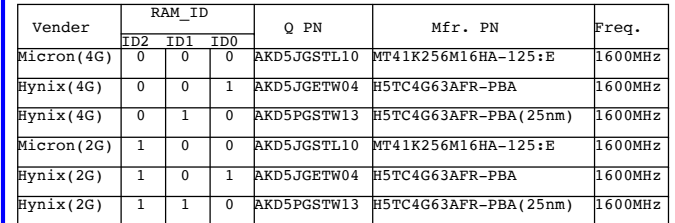
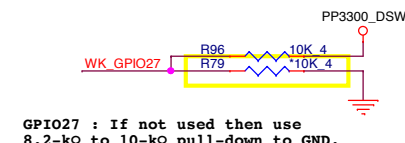




09



10



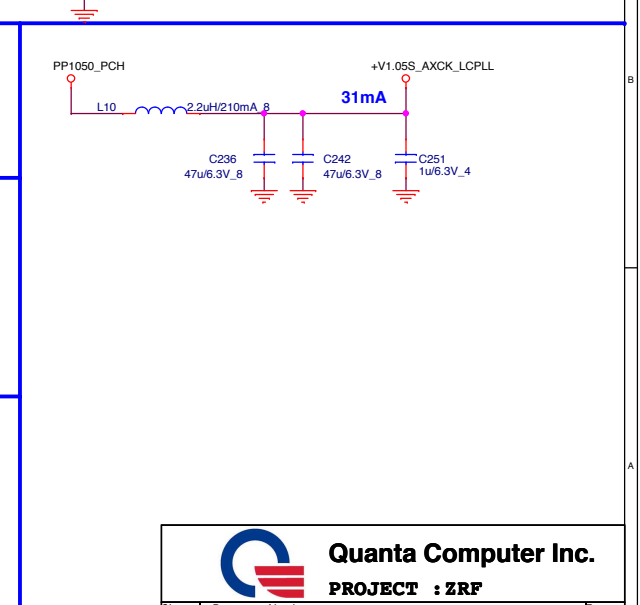
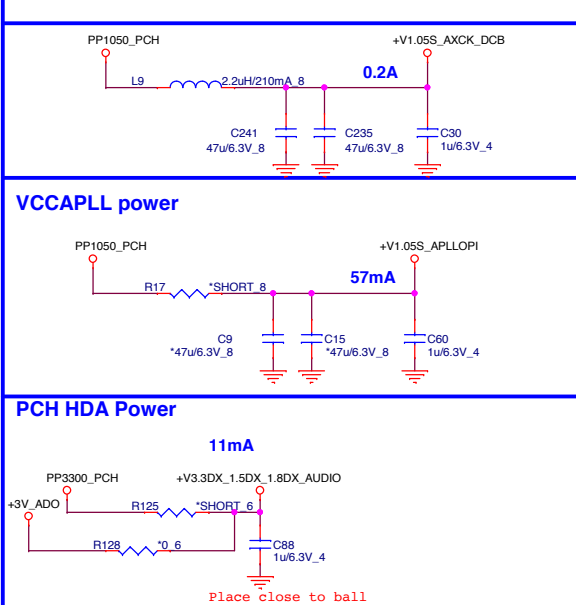
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**PROJECT : ZRF**

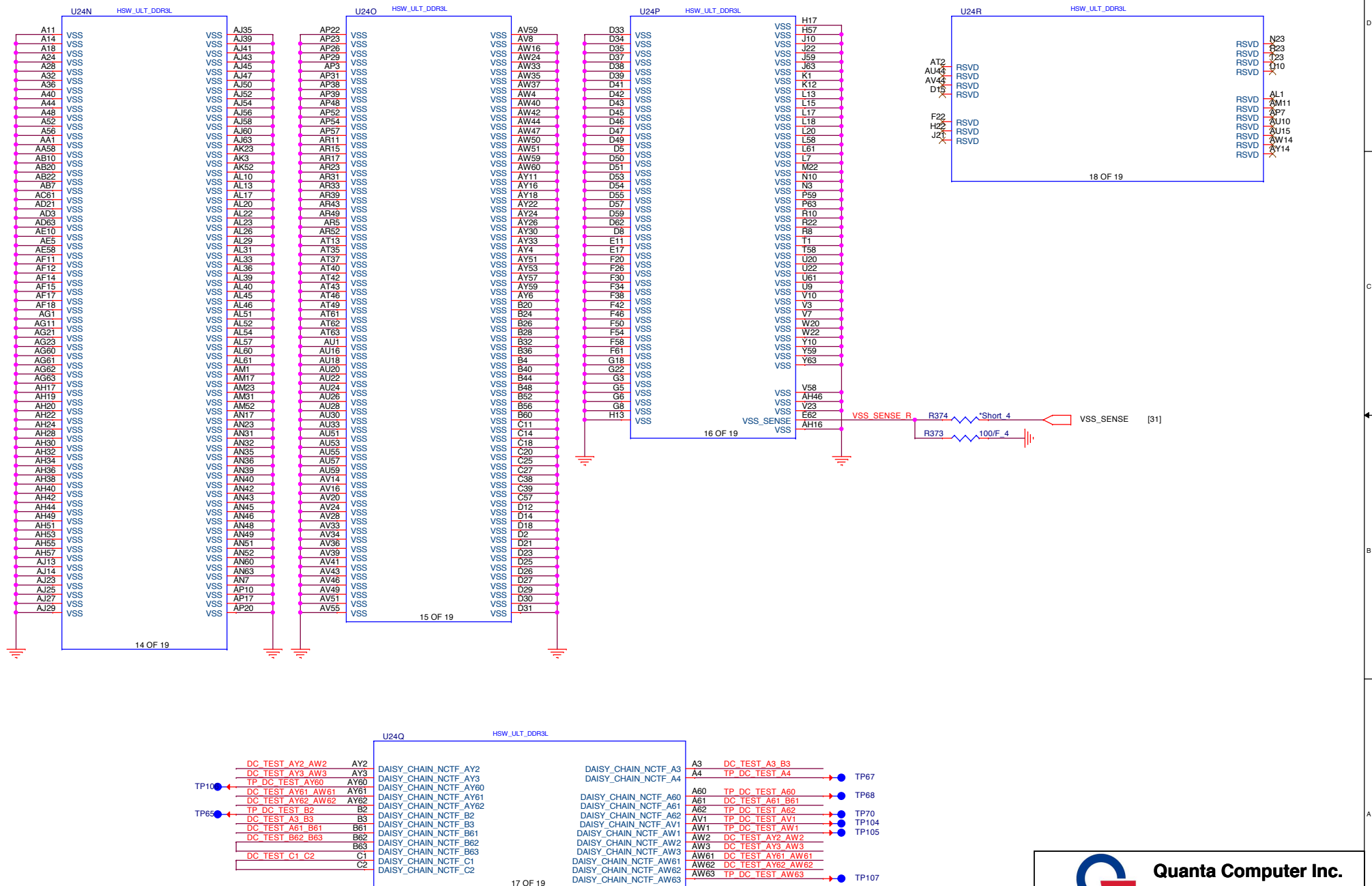
## Port Number

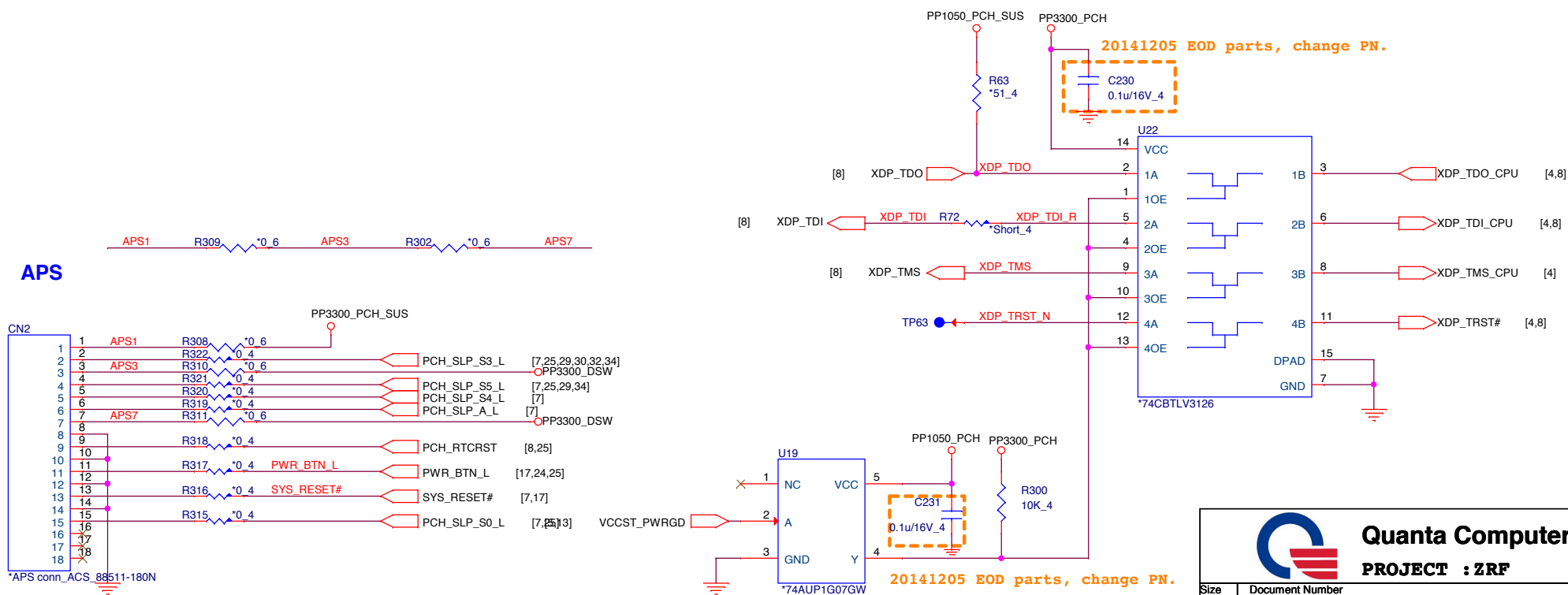
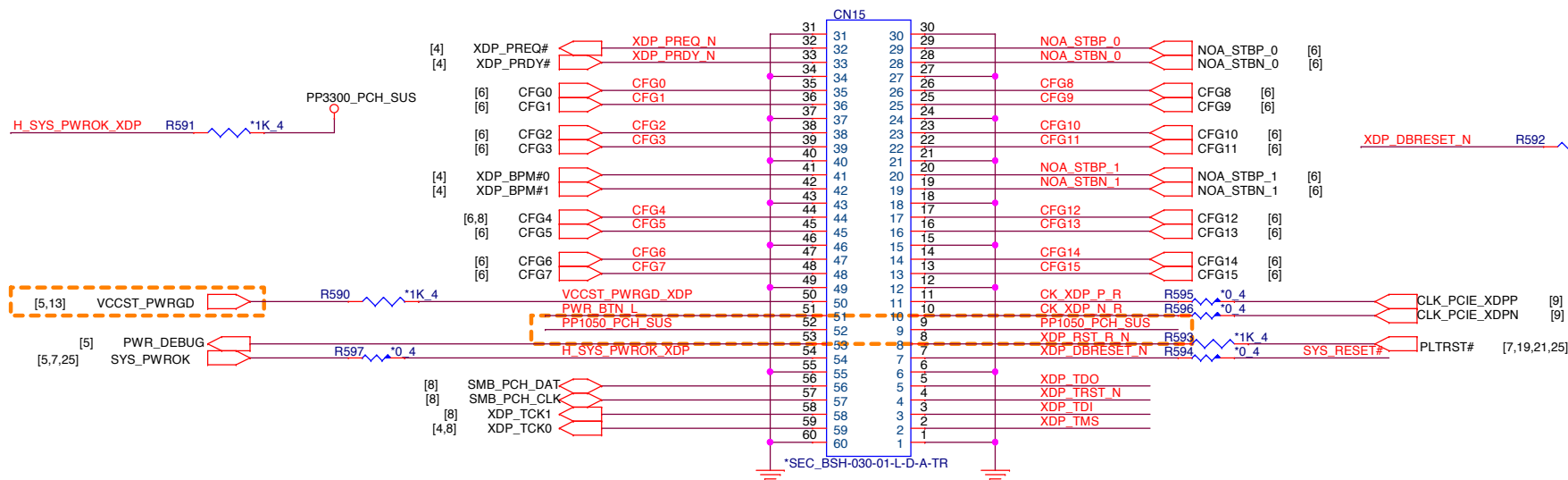
### PCH 4/6 (GPIO/MISC)

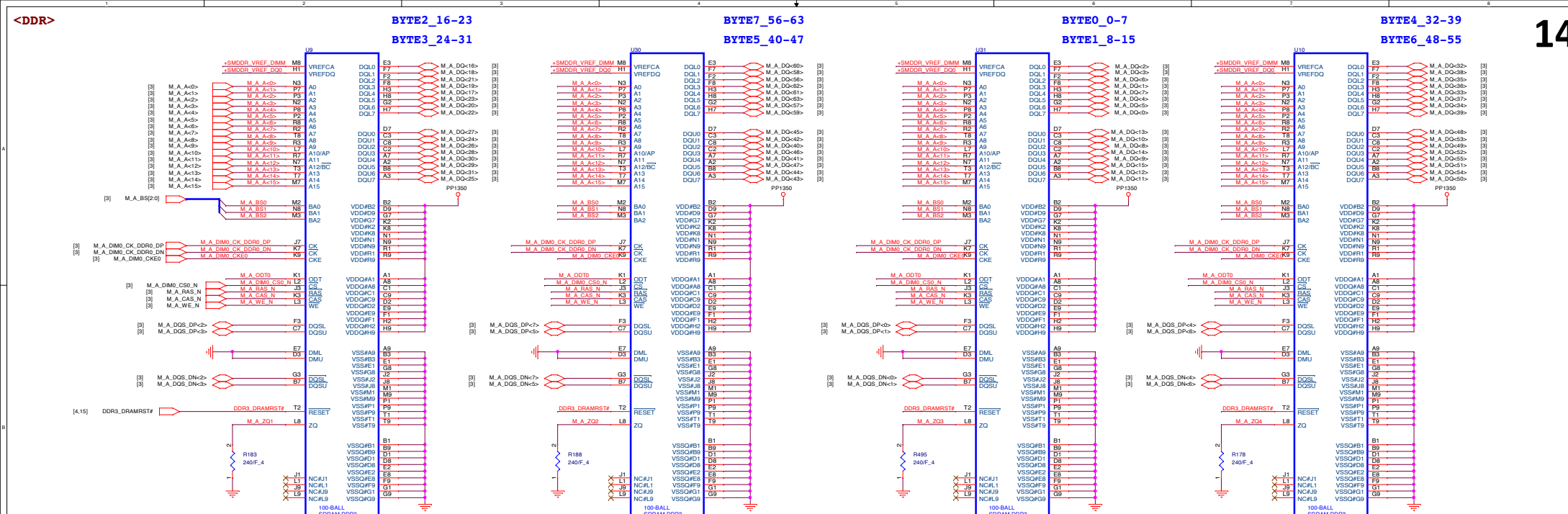
Size	Document Number	Rev
	<b>PCH 4/6 (GPIO/MISC)</b>	<b>A</b>
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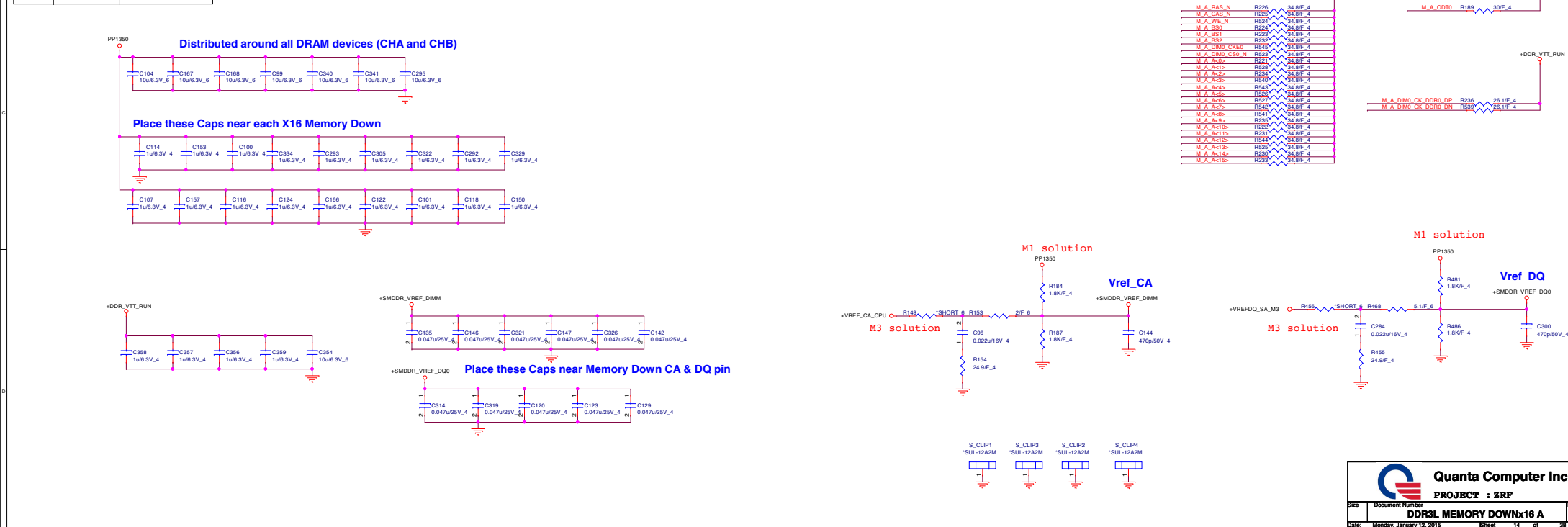


**Haswell ULT (GND)**

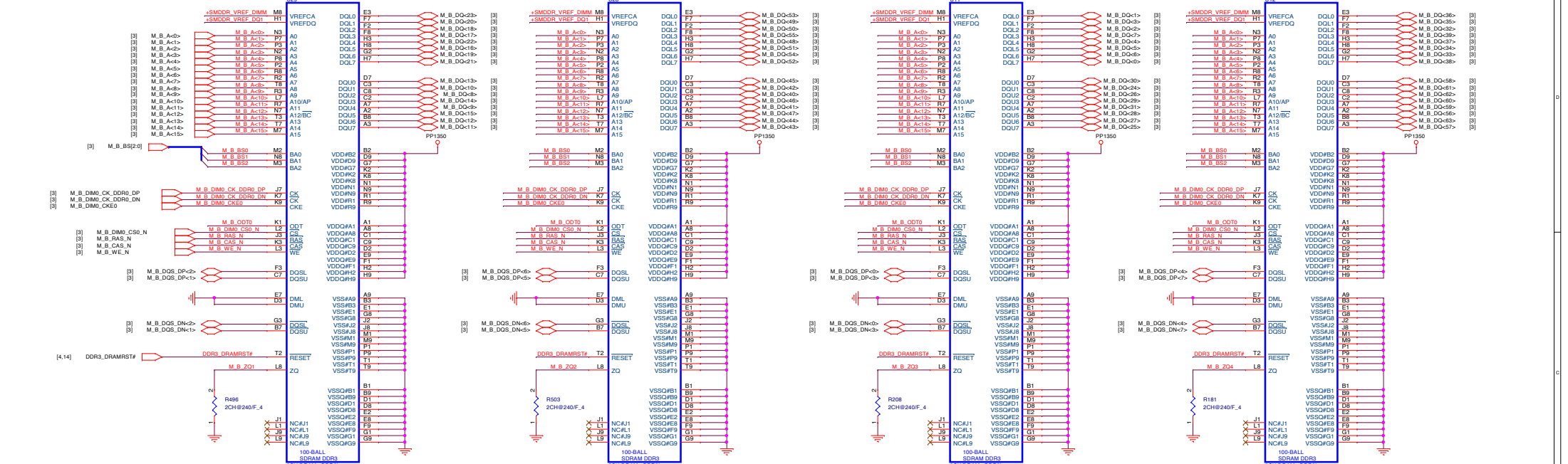




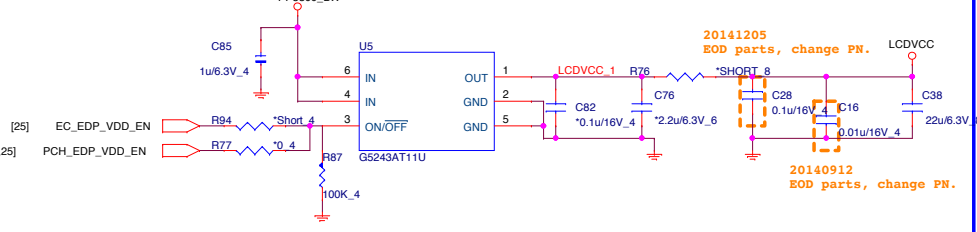
Vendor	P/N	
Hynix		
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1600Mhz 4Gb



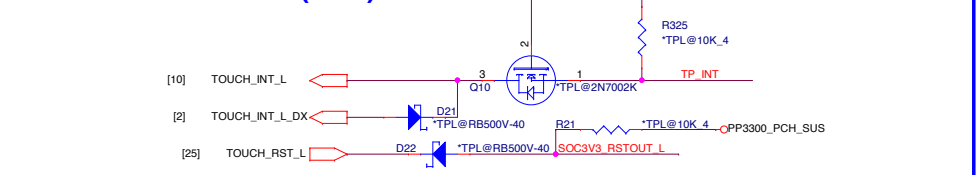




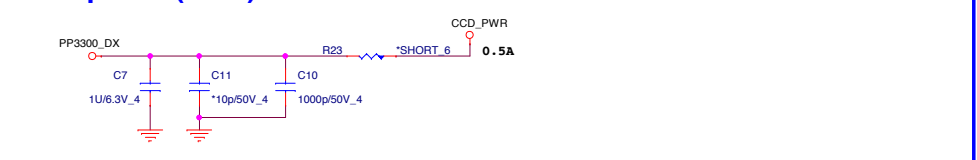
LVDS Power(LDS)



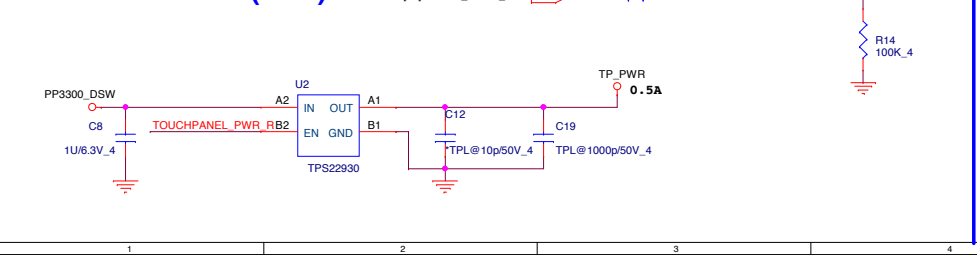
Touch Panel INT/RST(TSN)



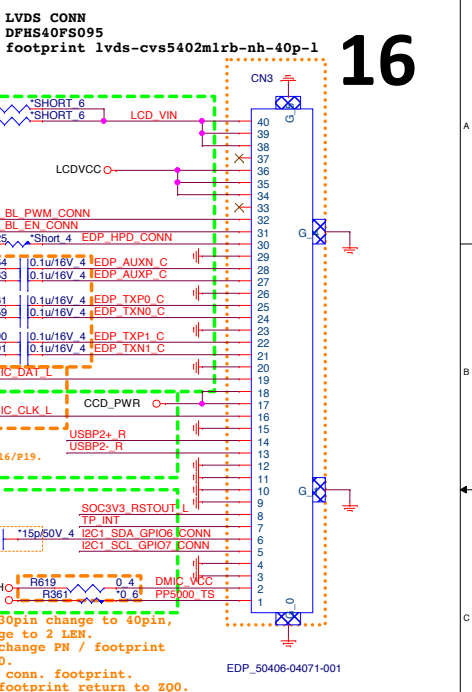
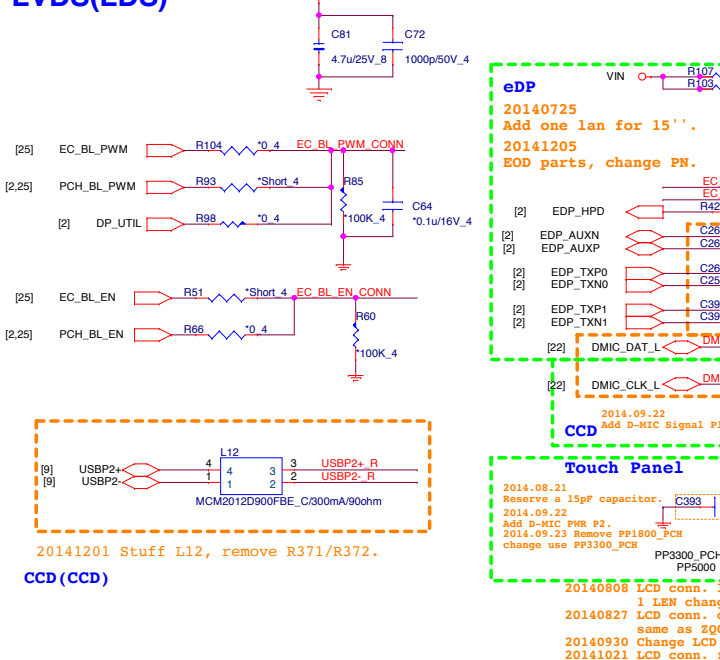
CCD power(CCD)



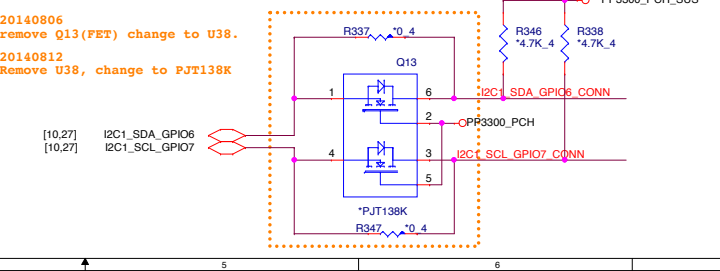
Touch Pad Power(TPD)



LVDS(LDS)

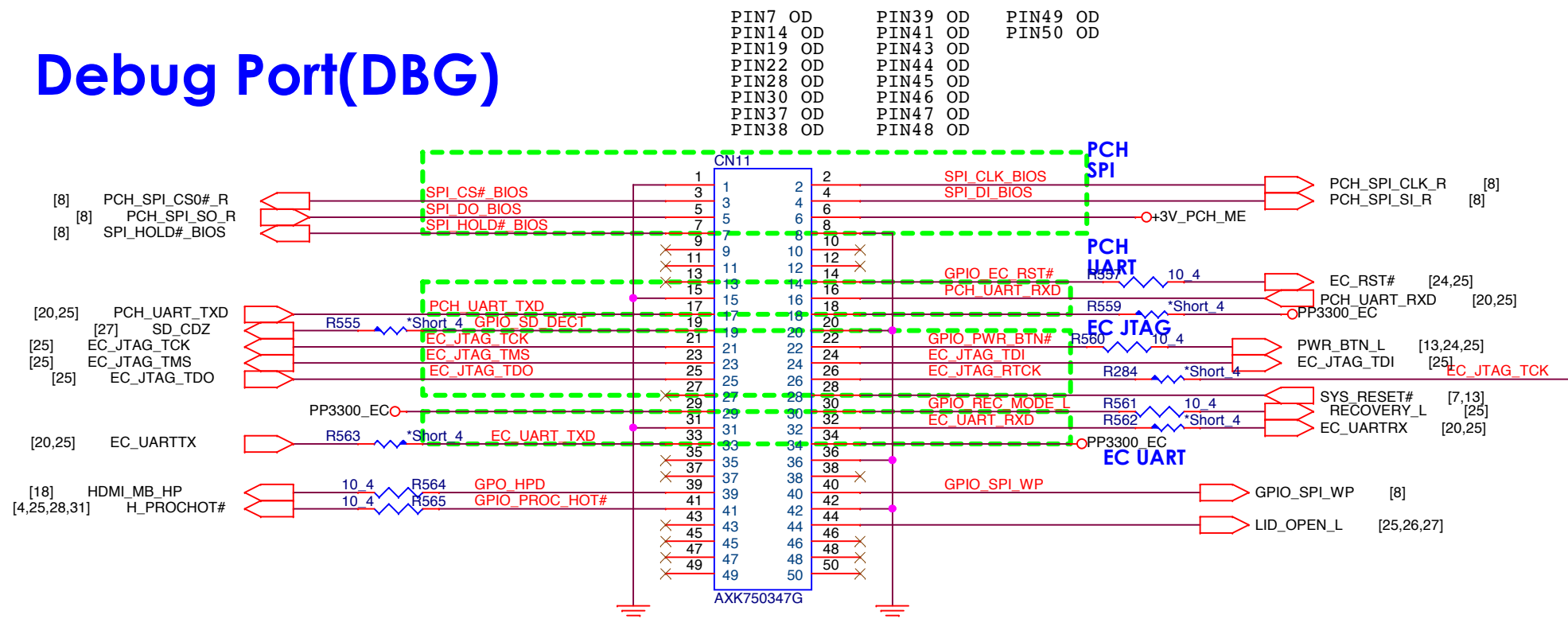


Touch Panel level shift(TSN)





# Debug Port(DBG)

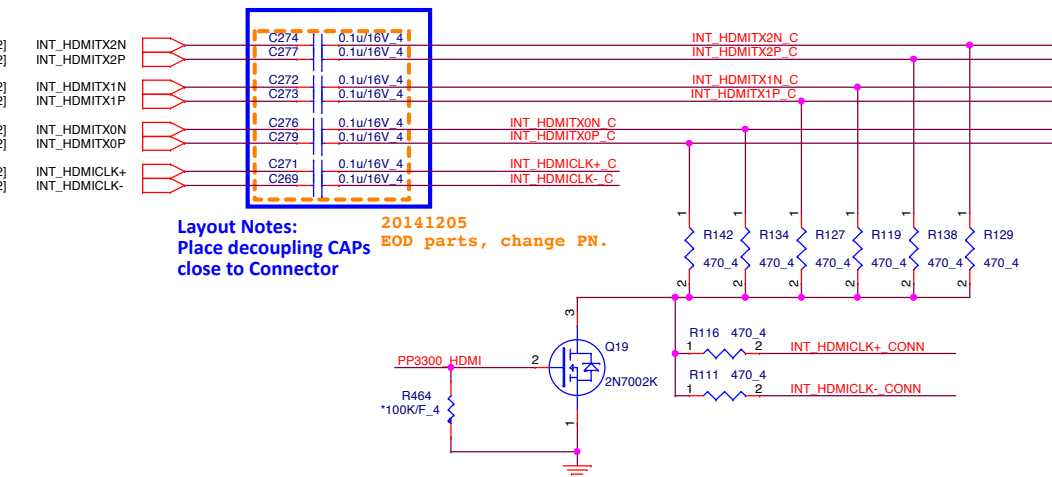


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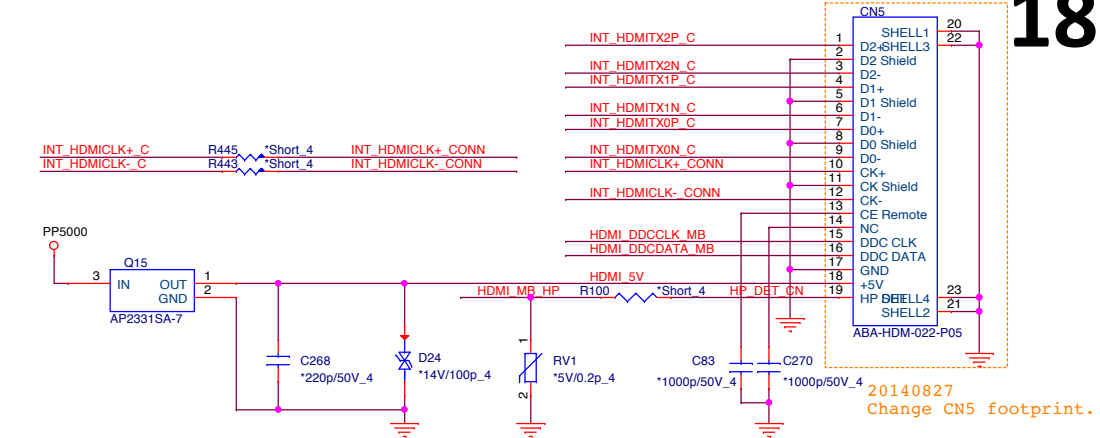
**PROJECT : ZRF**

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<b>Google Debug</b>		
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## HDMI Cost Reduced level shift (HDM)

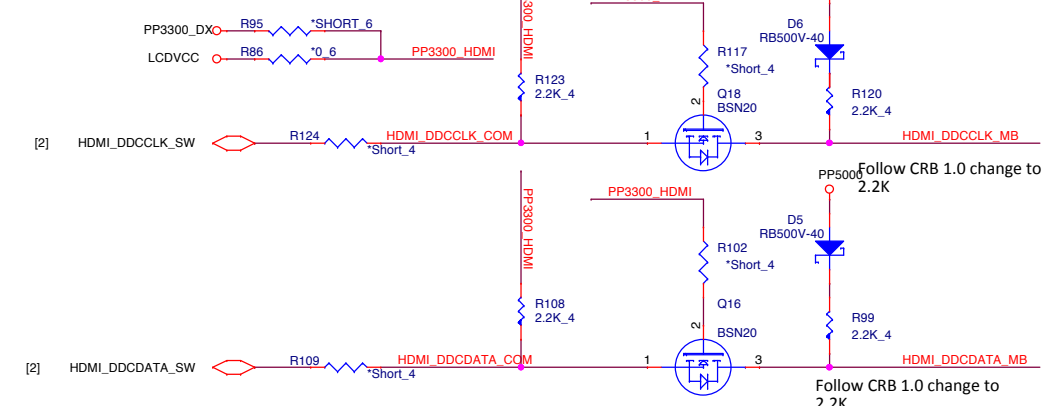


## HDMI connector (HDM)

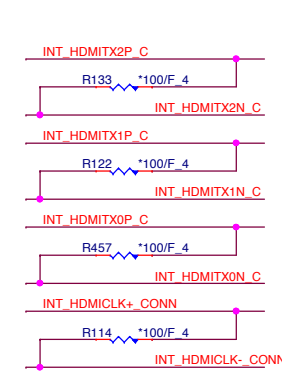


18

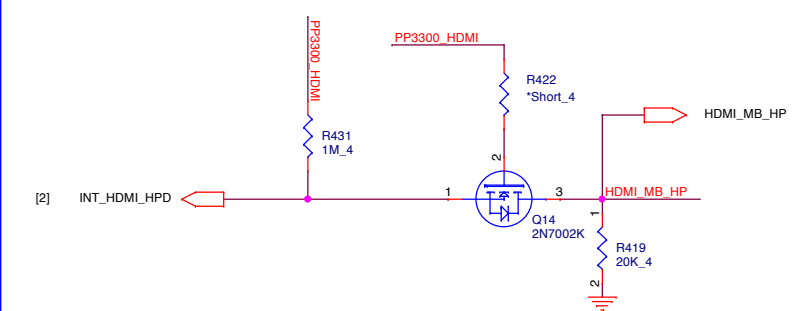
## HDMI DDC (HDM)



## EMI (HDM)



## HDMI-detect (HDM)

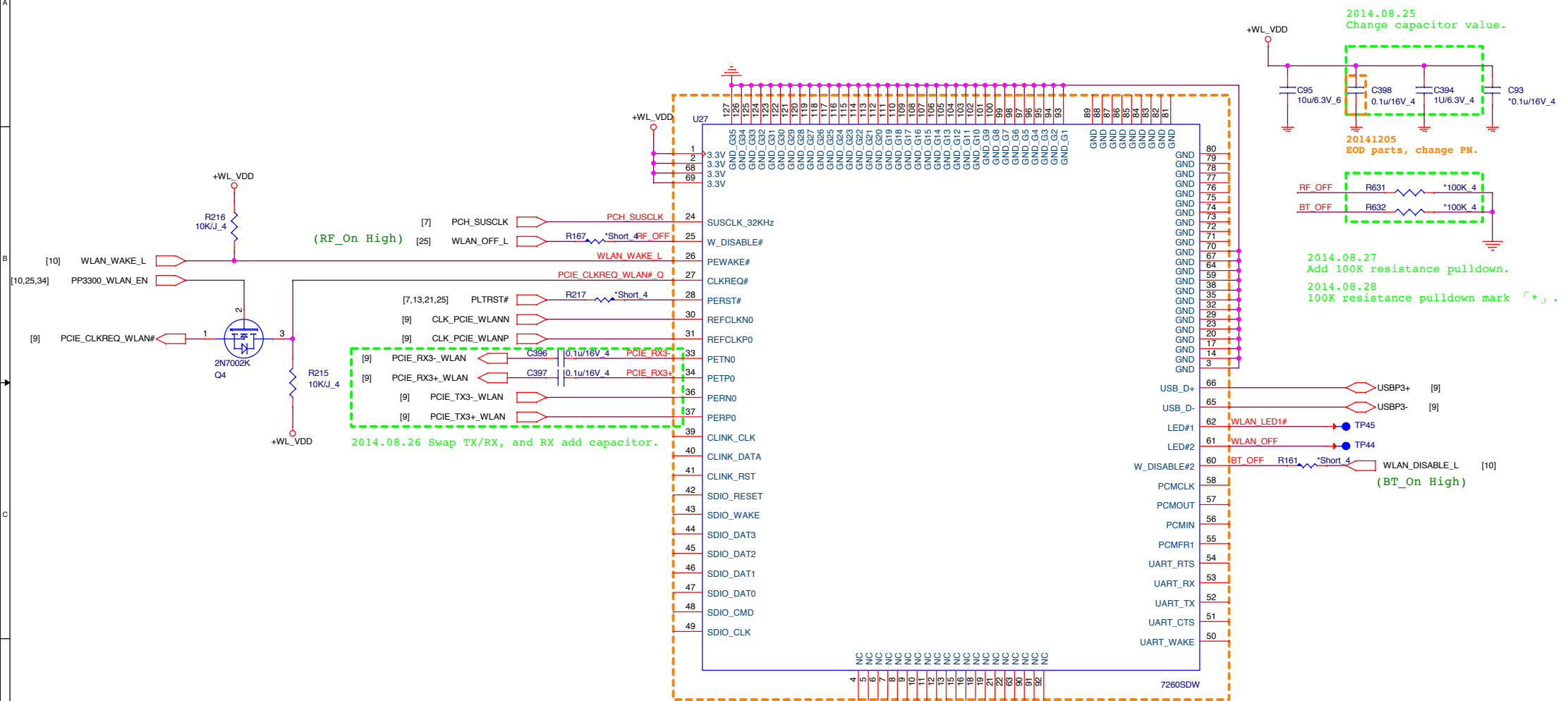


**Quanta Computer Inc.**


**PROJECT : ZRF**

**HDMI**

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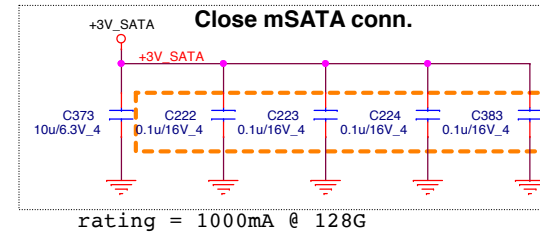


- 20140820 On board IC change to same as ZS8 connector
- 20140822 Return to another wifi onboard module 7260SDW
- 20140826 Change wifi onboard module 7260SDW footprint
- 20140909 Change wifi onboard module 7260SDW footprint
- 20141014 Change wifi onboard module 7260SDW PN.

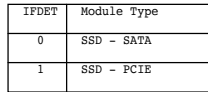


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**PROJECT : ZRF**

Size	Document Number	Rev A
WIFI / BT		
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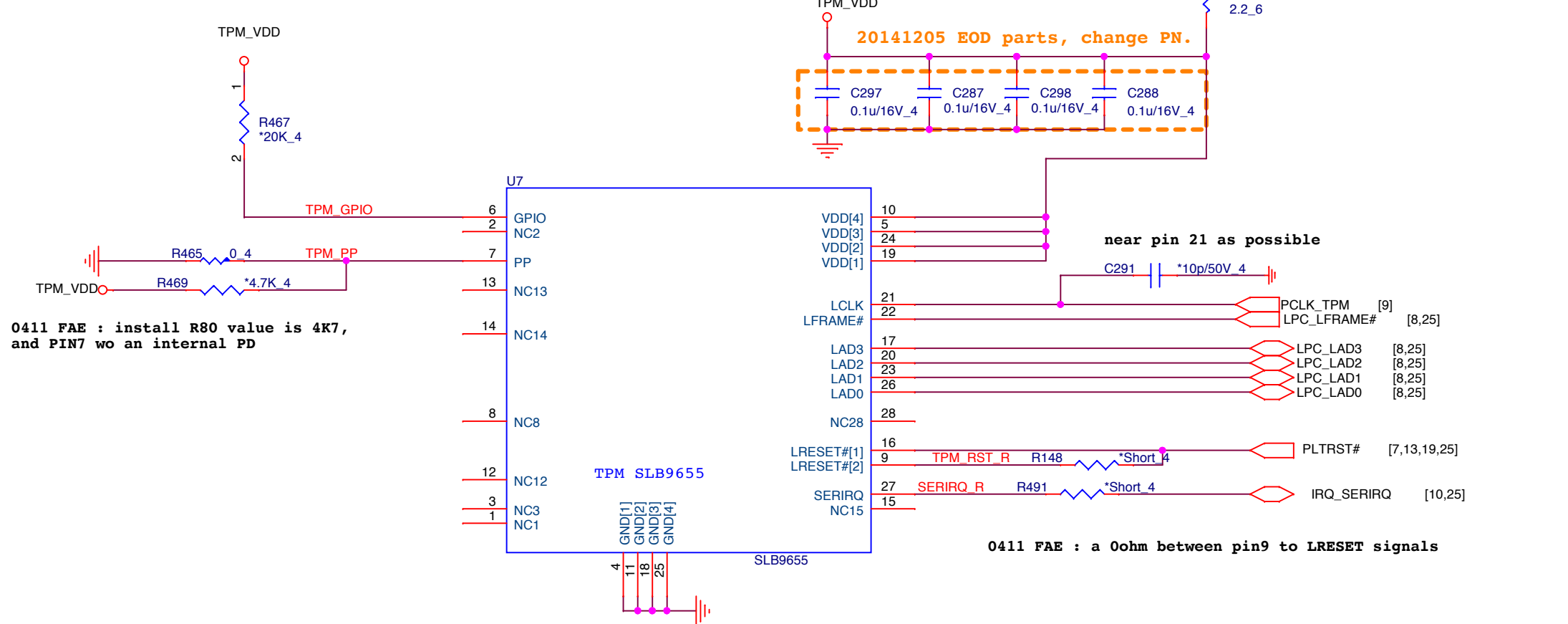


```
rating = 1000mA @ 128G
```



# TPM (TPM)

21

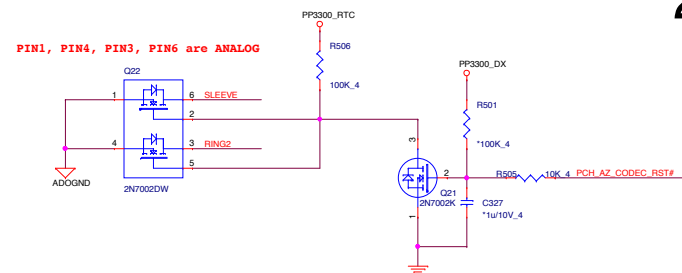


**Quanta Computer Inc.**  
**PROJECT : ZRF**

Size	Document Number	Rev A
<b>TPM SLB9655 / LED</b>		

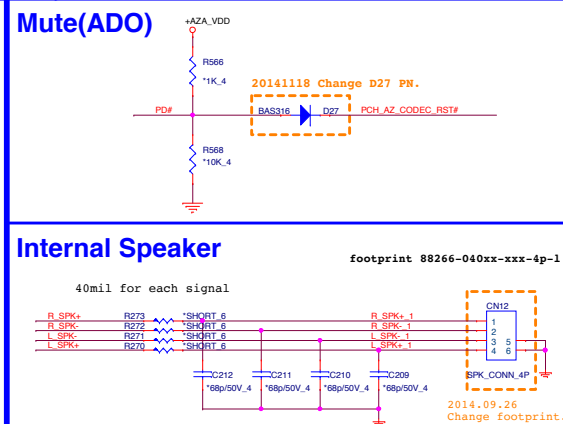
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22



20140922 Remove A-MIC, add D-MIC same as Hugo(ZHQ)

## Mute(ADO)

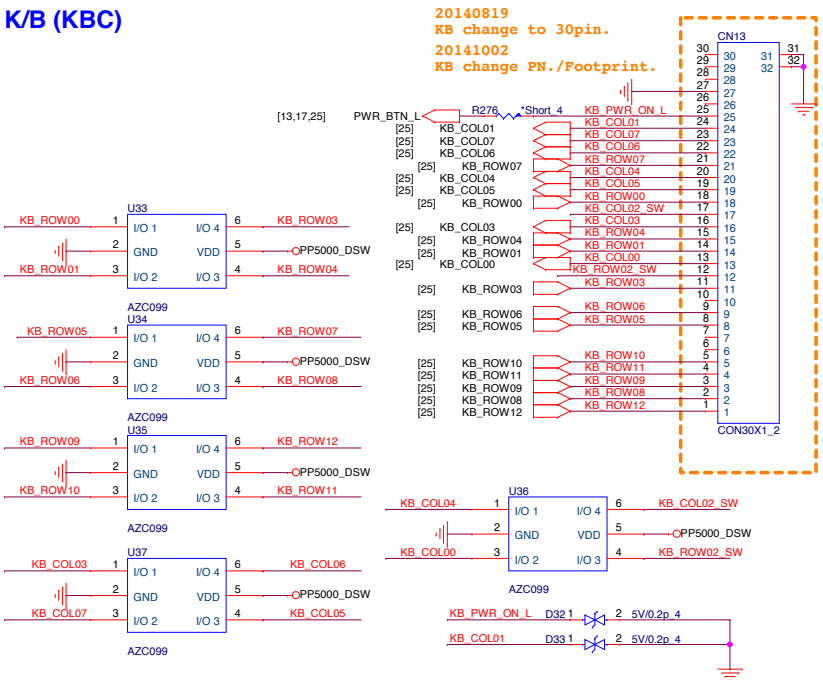


The schematic diagram illustrates the power plane layout, divided into digital and analog sections. The top section shows the digital power rail (PP1500\_PCH\_TS) connected to a 1.5A\_6 regulator, with a 10uF 3.3V capacitor (C201) and a 20140912 EOD parts change note. The bottom section shows the analog power rail (PP3300\_DX) connected to a 3.3V\_ADO regulator, with a 10uF 3.3V capacitor (C194) and a 20140912 EOD parts change note. The diagram also shows connections to +5V\_A, +3V\_ADO, and +3V\_AZA\_VDD.

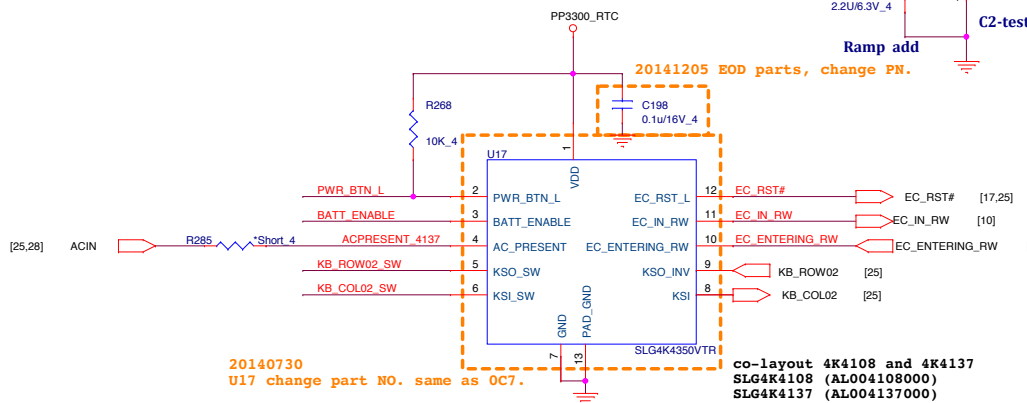
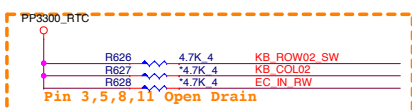
A vertical bar is divided into four segments labeled A, B, C, and D from bottom to top. An arrow points from the boundary between B and C to the right.



A

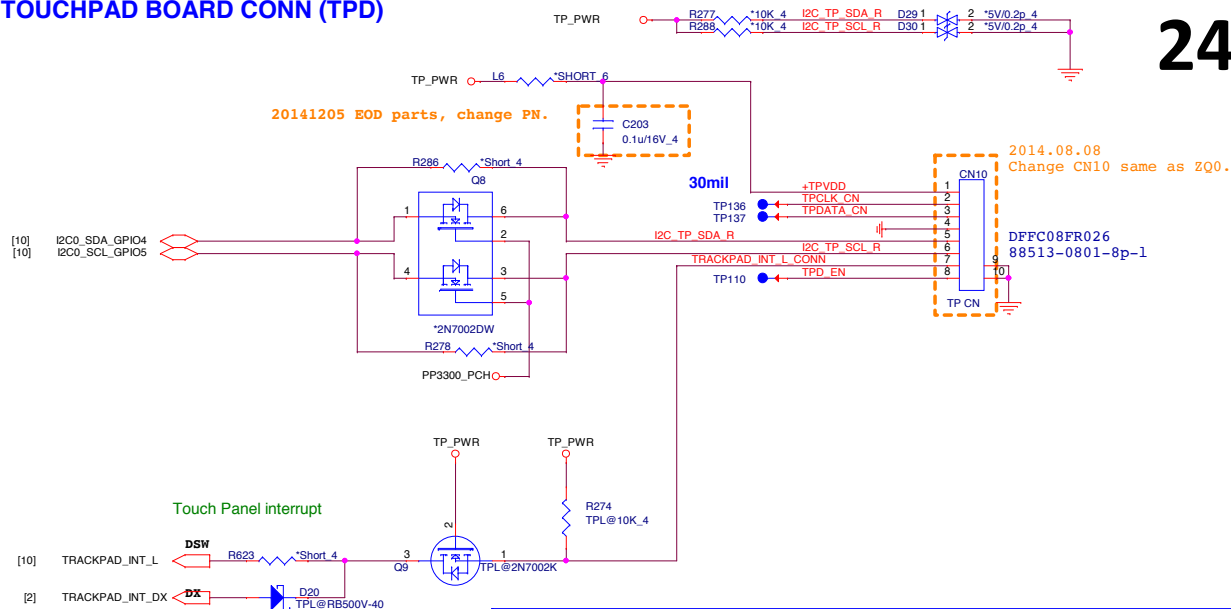


## HOLELESS RESET 2-CHIP(KBC)

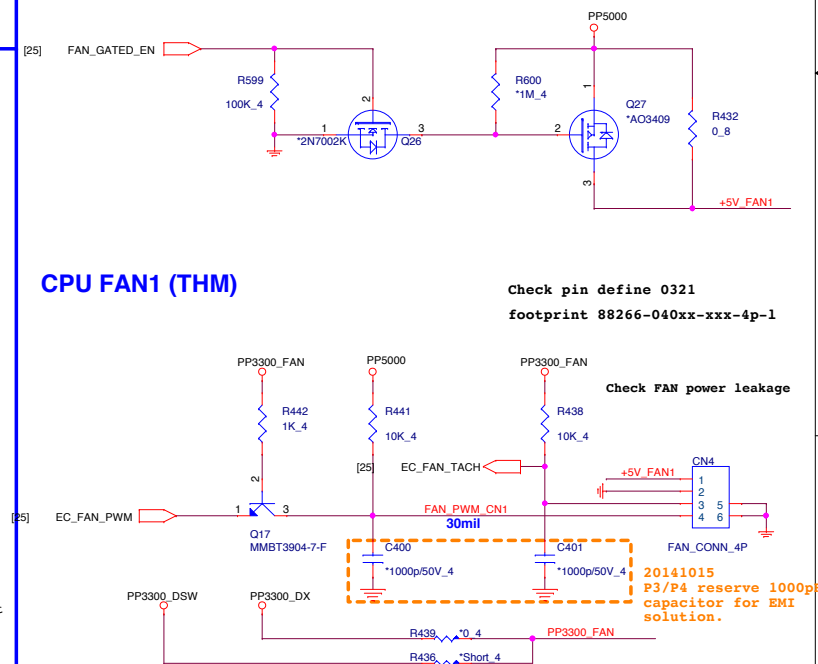


co-layout 4K4108 and 4K4137  
SLG4K4108 (AL004108000)  
SLG4K4137 (AL004137000)  
4K4137 PIN3 is BATT\_ENABLE  
4K4137 PIN4 is AC\_PRESENT

## TOUCHPAD BOARD CONN (TPD)



### CPU FAN1 (THM)



```

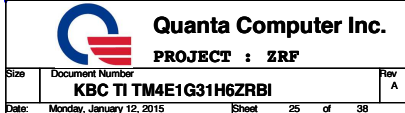
Check pin define 0321
footprint 88266-040xx-xxx-4p-1

```

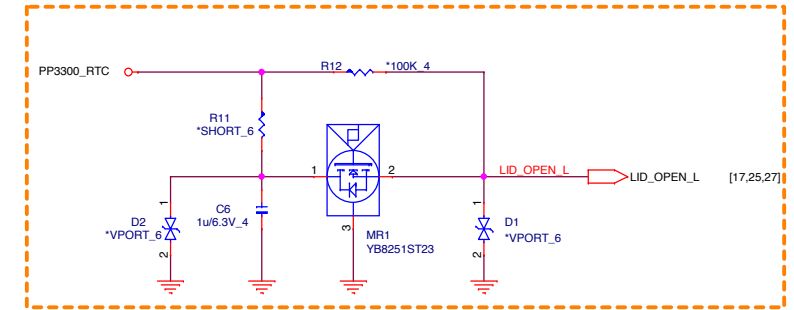
**Check FAN power leakage**

- 20141015
- P3/P4 reserve 1000pF
- capacitor for EMI solution.

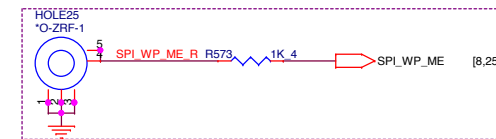




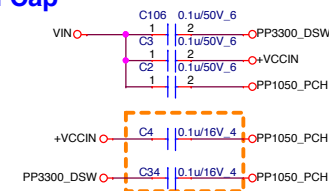
## Lid Switch (HSR)



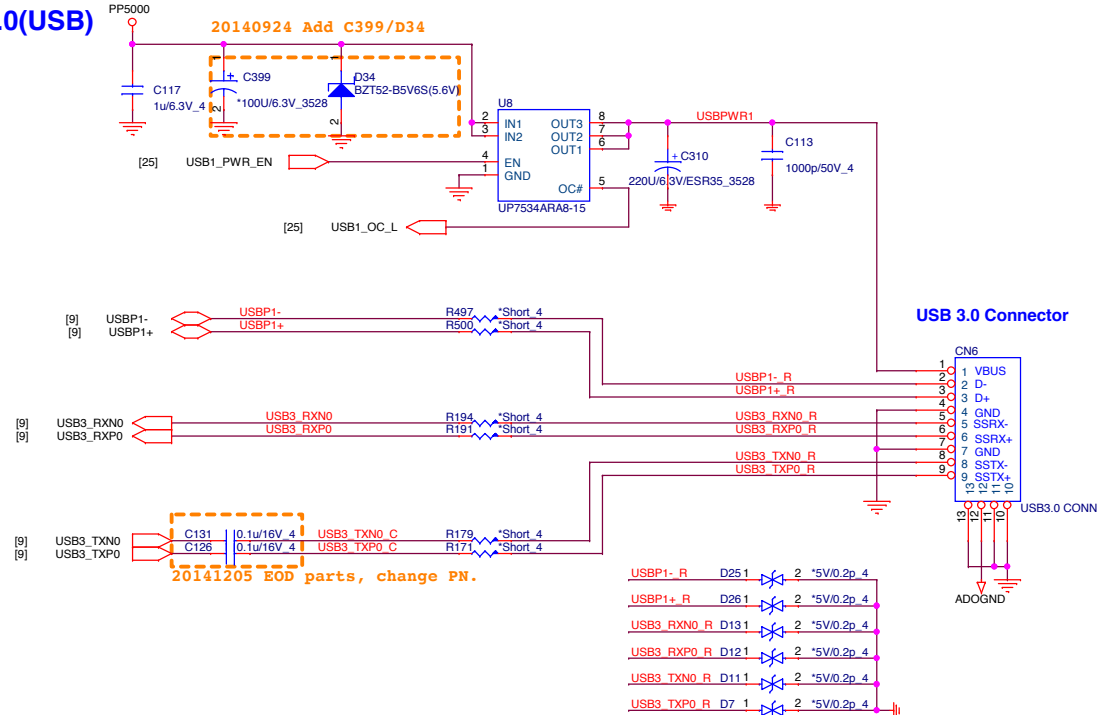
## 20140923 Add Lid Switch (HSR)



ROM WP#

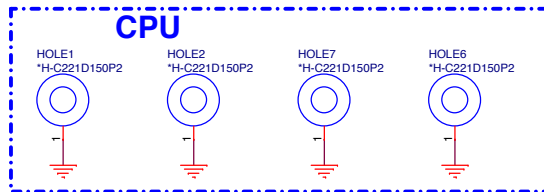
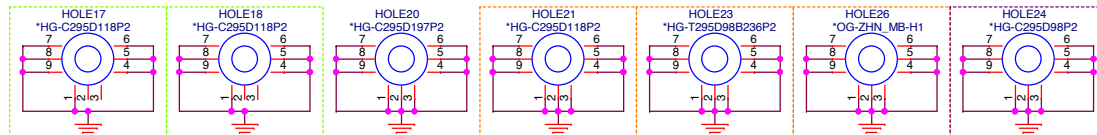


20141205 EOD parts, change PN.

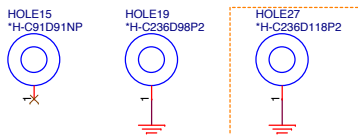


## USB3.0(USB)

## HOLE(OTH)



CPU



- ```
20140828
1. Add HOLE27
2. Change HOLE17/HOLE18/HOLE21/HOLE22
  /HOLE23/HOLE26 footprint
3. Remove HOLE9/HOLE16

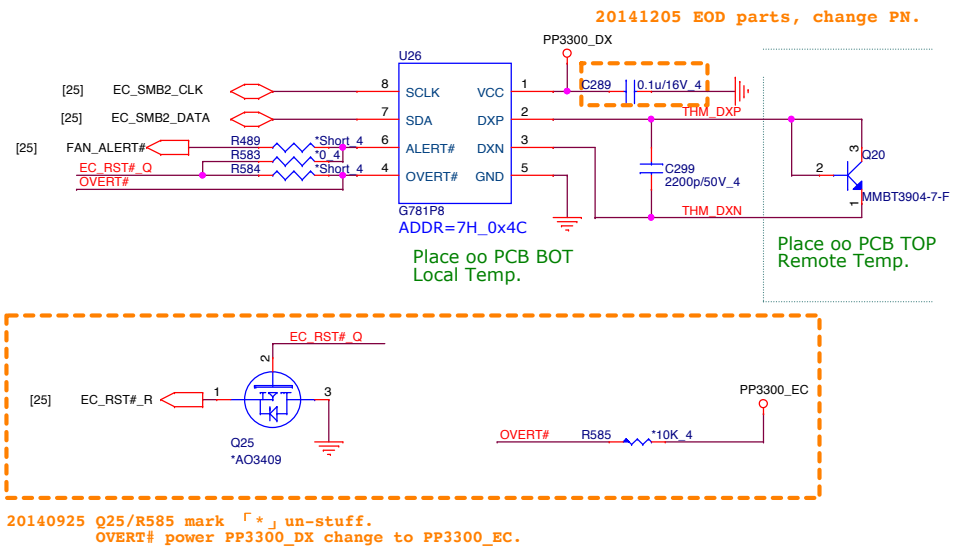
20140829
1. Change HOLE27 footprint
2. HOLE17/HOLE18/HOLE22 remove Pin1/Pin2/Pin3

20140901
1. Remove HOLE22

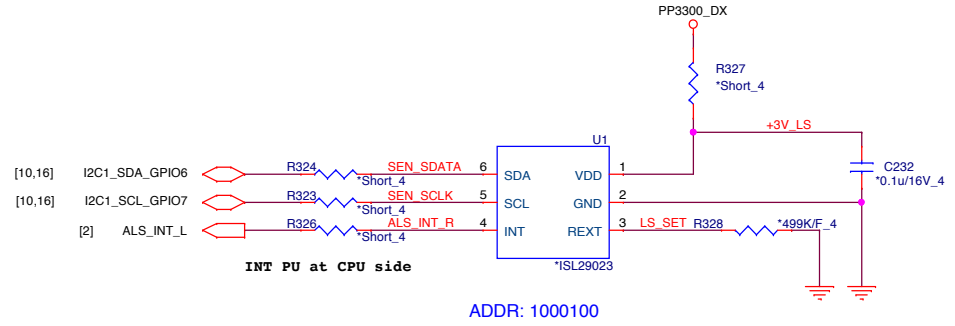
20140923
1. Remove battery enable, change to HOLE24

20140926
1. HOLE24 change footprint.
2. HOLE25 Add more 2pin & change footprint.
3. Remove HOLE3/4/5/8/10/11/12/13/14.
```

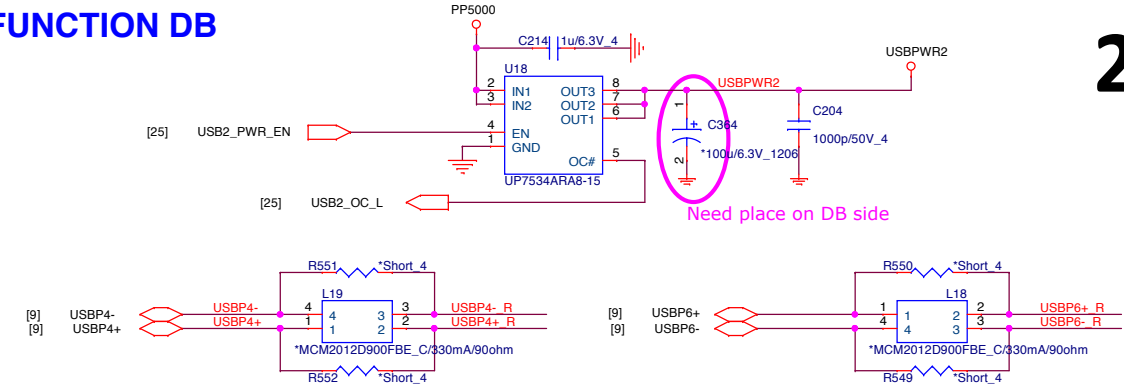
# Thermal Sensor(THM)



# Light sensor & TP (ALS)

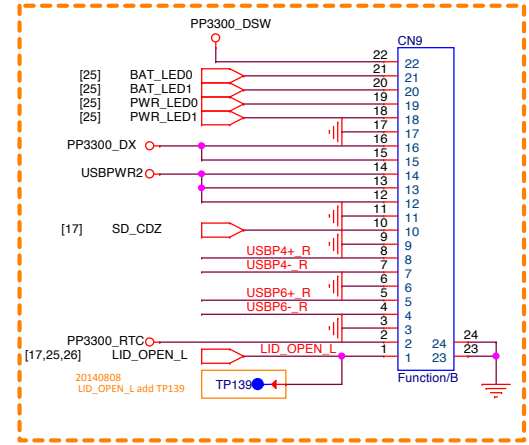



# FUNCTION DB



|     |            |
|-----|------------|
| HSR | +3VPCU     |
|     | LID_OPEN_L |
|     | GND        |
| LED | +3VPCU     |
|     | LED x 4    |
|     | GND        |
| USB | +3V x 2    |
|     | GND x 2    |
|     | USBP0+     |
|     | USBP0-     |
| CR  | CR_DET     |
|     | +3V x 2    |
|     | USBP6+     |
|     | USBP6-     |
|     | GND x 2    |
| LID | PP3300_RTC |
|     | LID_OPEN_L |

footprint 50501-0220n-v01-22p-1  
DFFC22FR019



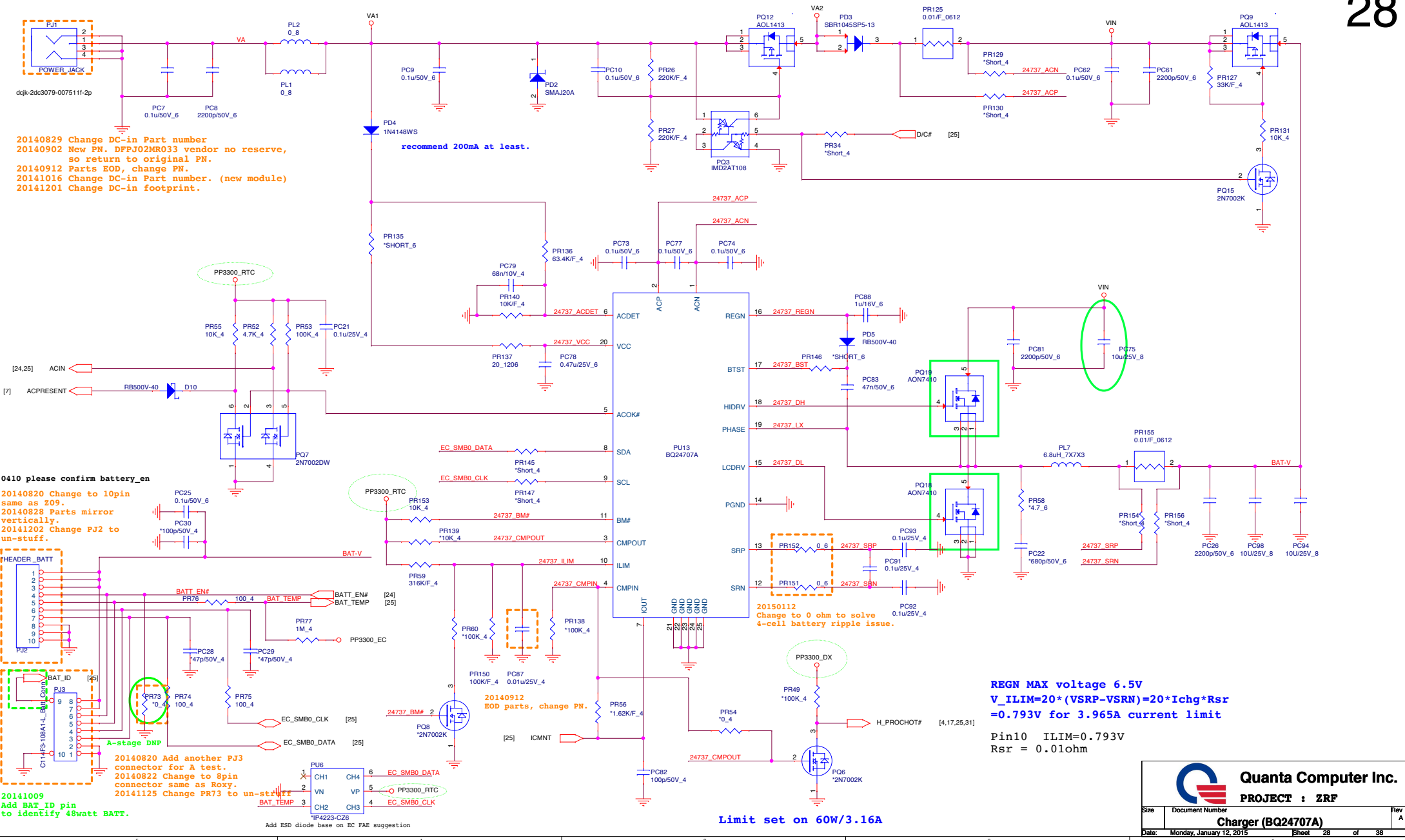
**Quanta Computer Inc.**  
**PROJECT : ZRF**

|       |                              |                |
|-------|------------------------------|----------------|
| Size  | Document Number              | Rev            |
|       | <b>DB/ALS/Thermal sensor</b> | <b>A</b>       |
| Date: | Monday, January 12, 2015     | Sheet 27 of 38 |

```

20140829 Change DC-in Part number
20140902 New PN. DFPJ02MR033 vendor no reserve,
          so return to original PN.
20140912 Parts EOD, change PN.
20141016 Change DC-in Part number. (new module)
20141201 Change DC-in footprint.

```




```

REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit

Pin10  ILIM=0.793V
Rsr = 0.01ohm

```

|                                                                                                                                           |                 |          |
|-------------------------------------------------------------------------------------------------------------------------------------------|-----------------|----------|
|  <b>Quanta Computer Inc.</b><br><b>PROJECT : ZRF</b> |                 | Rev<br>A |
| Size                                                                                                                                      | Document Number |          |
| <b>Charger (BQ24707A)</b>                                                                                                                 |                 |          |
| Date: Monday, January 12, 2015                                                                                                            | Sheet 28 of 38  |          |

TDC : 0.75A  
PEAK : 1A  
Width : 40mil

TDC : 0.38A  
PEAK : 0.5A  
Width : 20mil

+DDR\_VTT\_RUN

PR66 \*SHORT\_6

PC108  
10u/6.3V\_6

PC109  
10u/6.3V\_6

PP3300\_EC

PR164  
100K/F\_4

PP1350\_PGOOD

PR162  
\*Short\_4

PR78  
200K/F\_4

PR79  
61.9K/F\_4

VREF=1.8V

20141205 EOD parts, change PN.

PC101  
0.1u/16V\_4

PR81  
\*0\_4

PR68  
10K/F\_4

PR67  
30.1K/F\_4

PC100  
0.01u/25V\_4

20140912  
EOD parts, change PN.

Greater than or equal 40mil

PP5000\_DSW

PP5000

PR160  
\*Short\_4

PR159  
\*0\_4

PC104  
10u/6.3V\_6

PC103  
1u/10V\_4

PO21  
AON7410

PC105  
0.1u/50V\_6

PR161  
2/F\_6

PC106  
2200p/50V\_4

PC31  
10u/25V\_8

PL9  
3.3uH\_7X7X3

PR72  
\*4.7\_6

PC27  
\*680p/50V\_6

PC107  
0.1u/50V\_6

PC99  
330u/2V\_7343

Close to output cap

1.35 Volt +/- 5%  
TDC : 3.35A  
PEAK : 4.46A  
OCP : 6A  
Width : 140mil

| Mode | Frequency | Discharge mode     |
|------|-----------|--------------------|
| 200K | 400K      | Tracking Discharge |
| 100K | 300K      | Tracking Discharge |

|                  | S3 | S5 | +1.35VSUS | REF | VTT |
|------------------|----|----|-----------|-----|-----|
| S0               | 1  | 1  | ON        | ON  | ON  |
| S3 (main on off) | 0  | 1  | ON        | ON  | OFF |
| S4/S5            | 0  | 0  | OFF       | OFF | OFF |

OCP=6A  
L ripple current  
= $(19-1.35) \times 1.35 / (3.3 \mu \times 400 \times 19)$   
=0.95A  
Vtrip=[ $6 - (0.95/2)$ ]\*14mohm  
=0.07735V  
Rlimit= $0.07335 / 10 \mu \text{A} \times 8 = 61.88 \text{Kohm}$

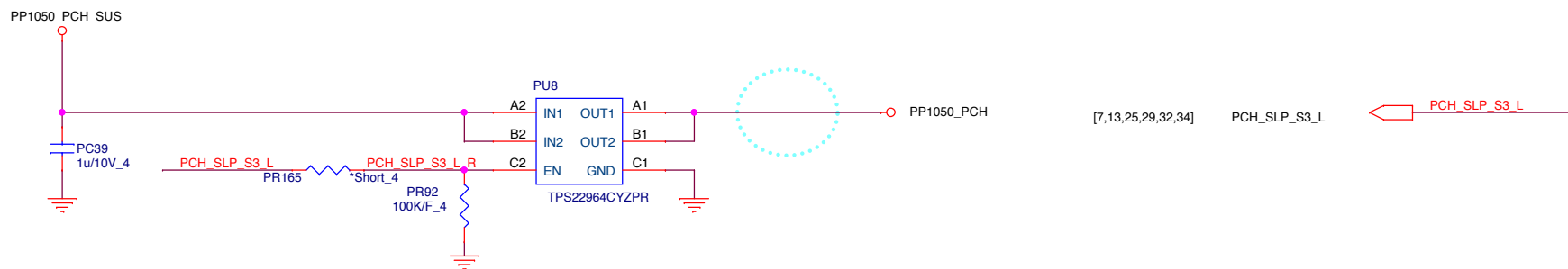
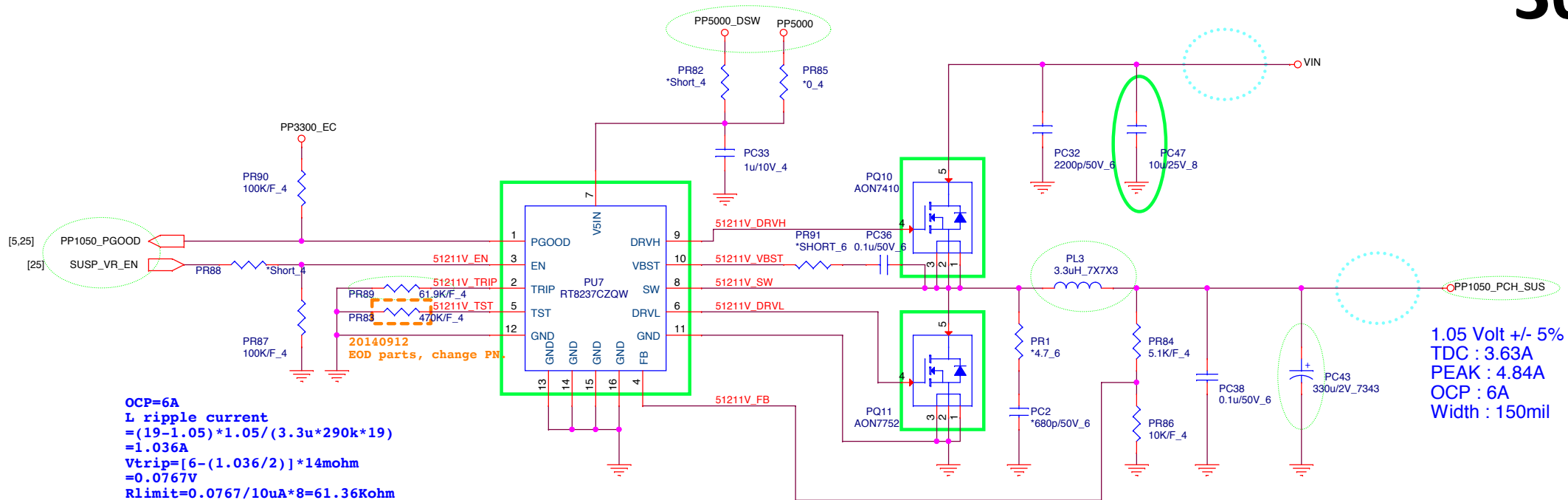


Quanta Computer Inc.

PROJECT : ZRF

| Size | Document Number   | Rev |
|------|-------------------|-----|
|      | DDR 1.35V (G5316) | A   |

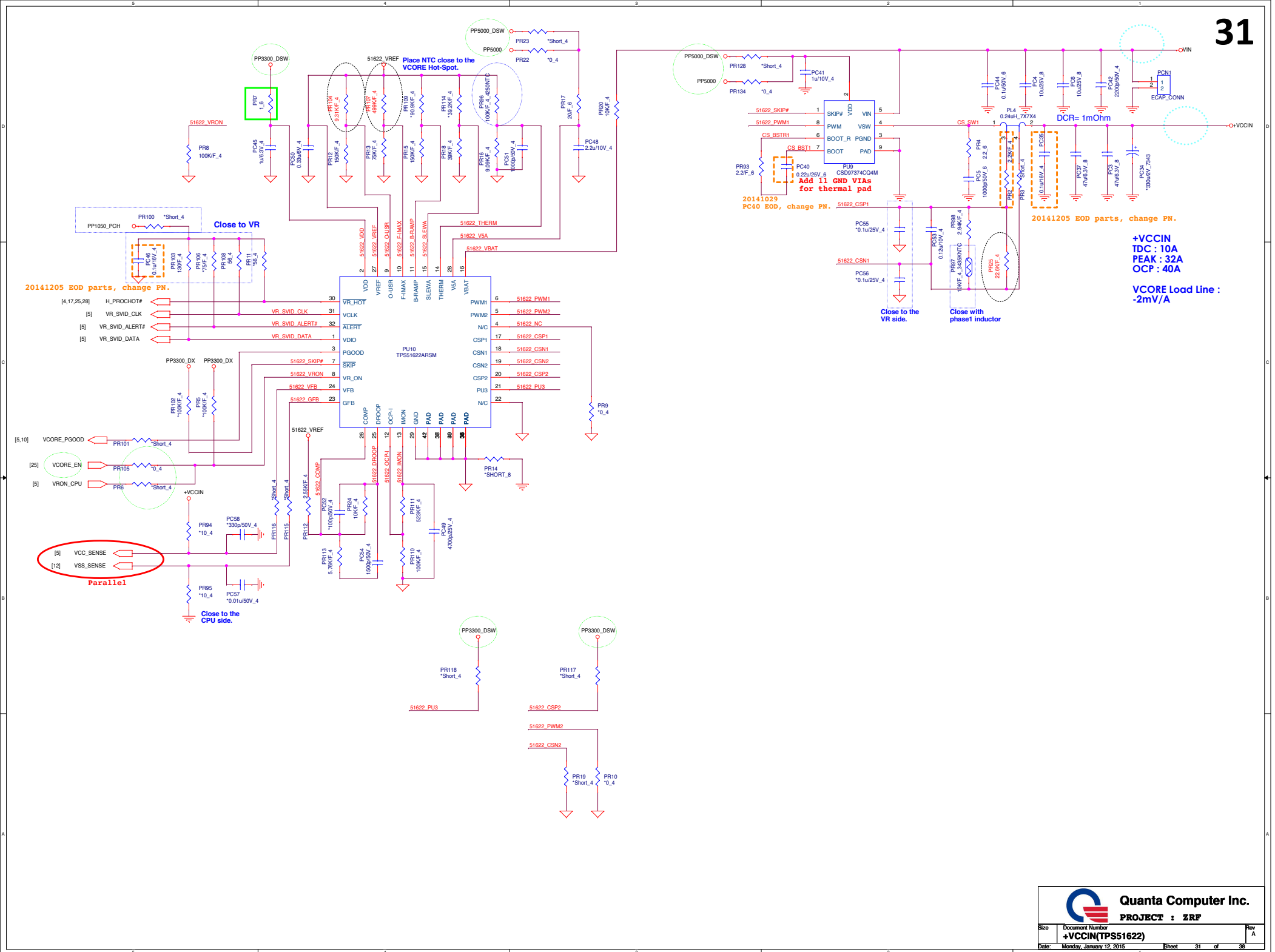
Date: Monday, January 12, 2015 Sheet 29 of 38

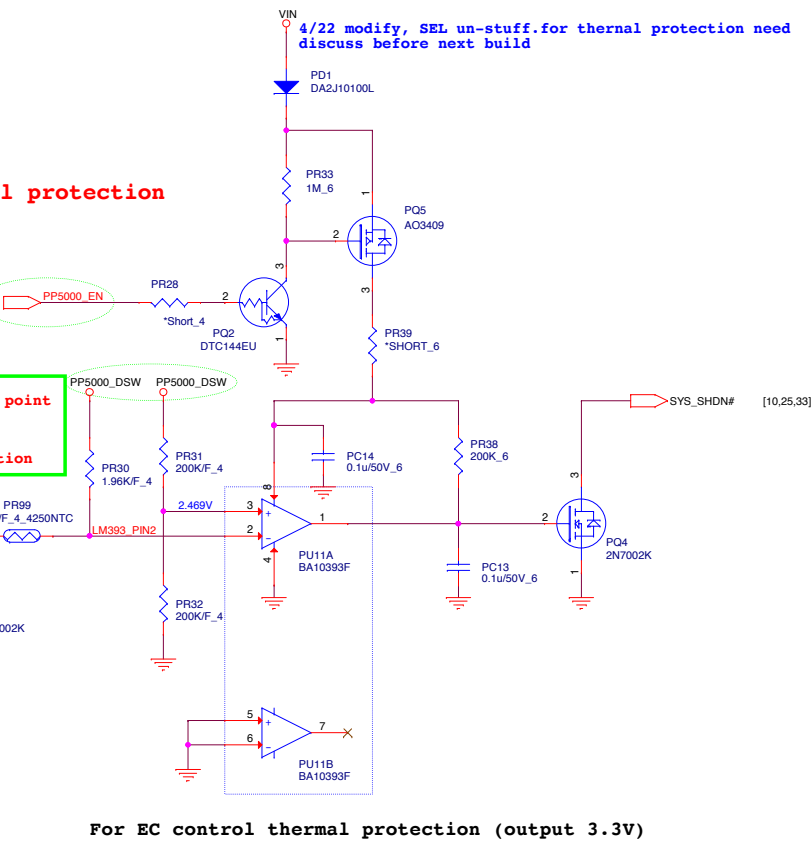
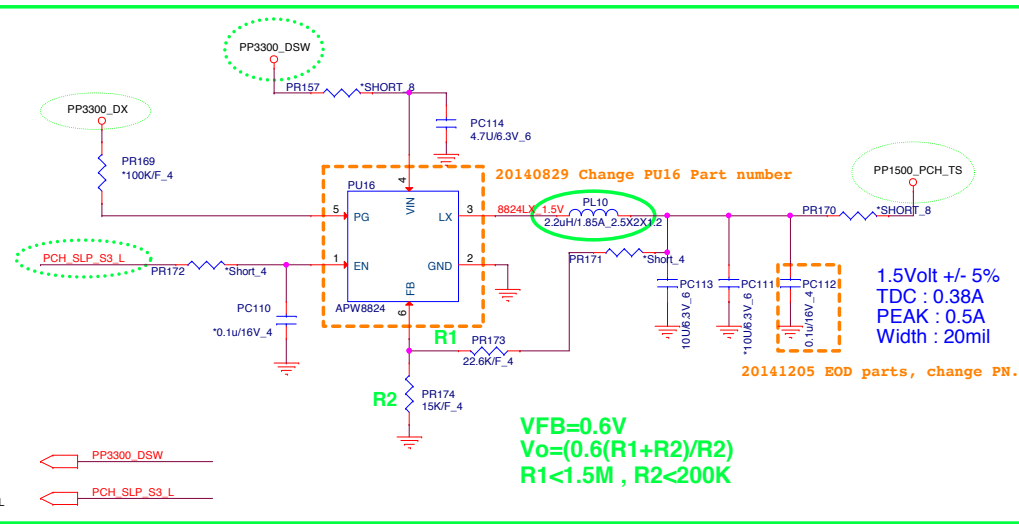


**Quanta Computer Inc.**  
**PROJECT : ZRF**

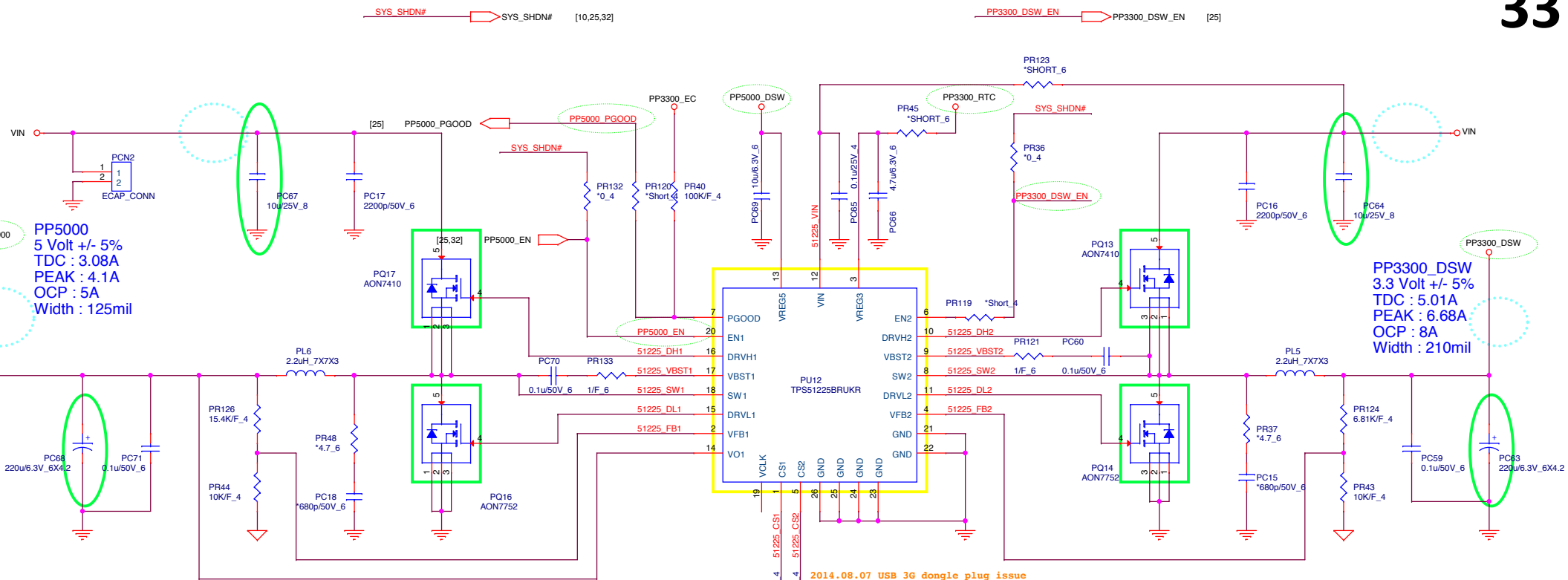
| Size | Document Number        | Rev      |
|------|------------------------|----------|
|      | <b>+1.05V (RT8237)</b> | <b>A</b> |

Date: Monday, January 12, 2015 Sheet 30 of 38





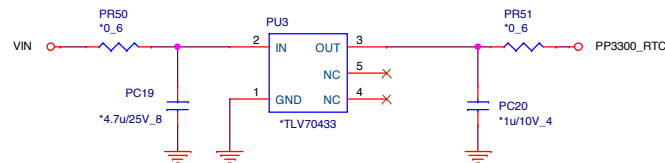



**OCP:5A**


$L(\text{ripple current}) = (9-5) \cdot 5 / (2.2 \mu \cdot 0.3 \text{M} \cdot 9) = 3.367 \text{A}$   
 $I_{\text{ocp}} = 5 - (3.367/2) = 3.316 \text{A}$   
 $V_{\text{th}} = (3.316 \text{A} \cdot 14 \text{m}\Omega) + 1 \text{mV} = 47.43 \text{mV}$   
 $R(\text{Ilim}) = (47.43 \text{mV} \cdot 8) / 10 \mu \text{A} = 37.94 \text{K}$


**OCP:8A**

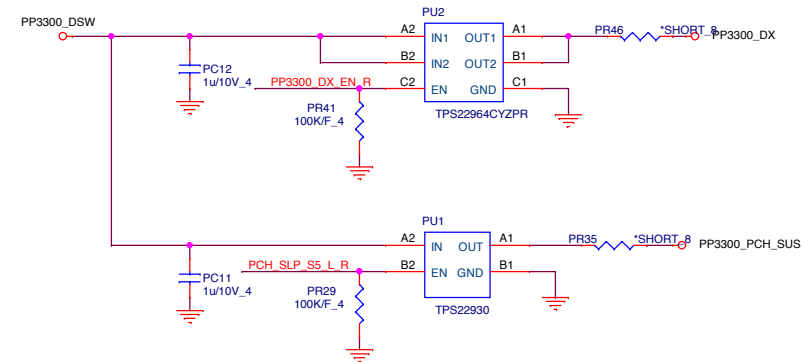
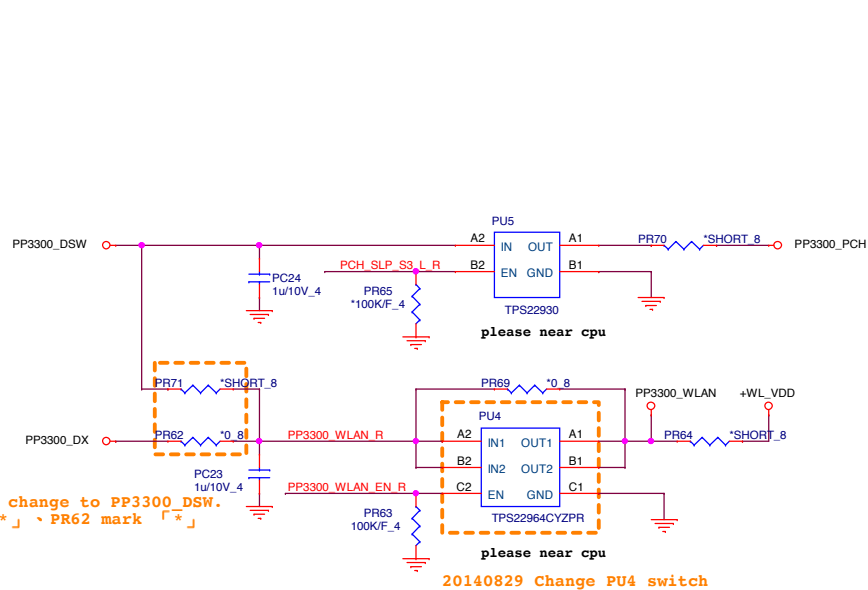
$L(\text{ripple current}) = (9-3.3) \cdot 3.3 / (2.2 \mu \cdot 0.355 \text{M} \cdot 9) \sim 2.676 \text{A}$   
 $I_{\text{ocp}} = 8 - (2.676/2) = 6.662 \text{A}$   
 $V_{\text{th}} = (6.662 \text{A} \cdot 14 \text{m}\Omega) + 1 \text{mV} = 94.27 \text{mV}$   
 $R(\text{Ilim}) = (94.27 \text{mV} \cdot 8) / 10 \mu \text{A} = 75.41 \text{K}$



[7,13,25,29,30,32] PCH\_SLP\_S3\_L  PCH\_SLP\_S3\_L PR166 \*Short\_4 PCH\_SLP\_S3\_L\_R

[25] PP3300\_DX\_EN  PP3300\_DX\_EN PR167 \*Short\_4 PP3300\_DX\_EN\_R

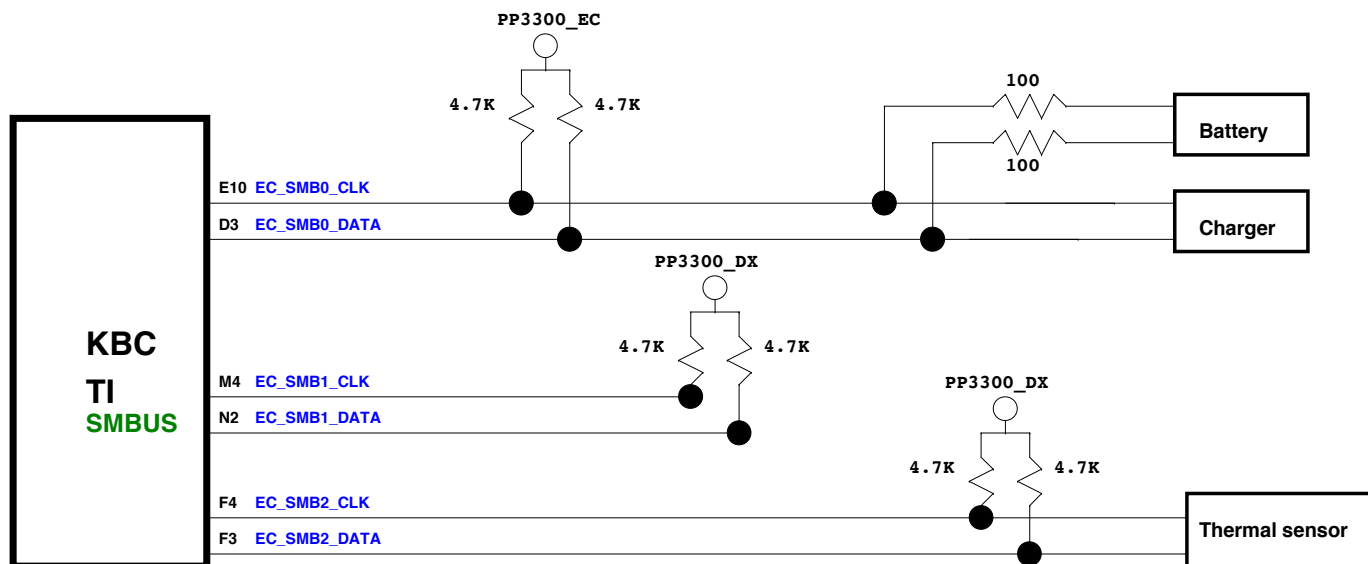
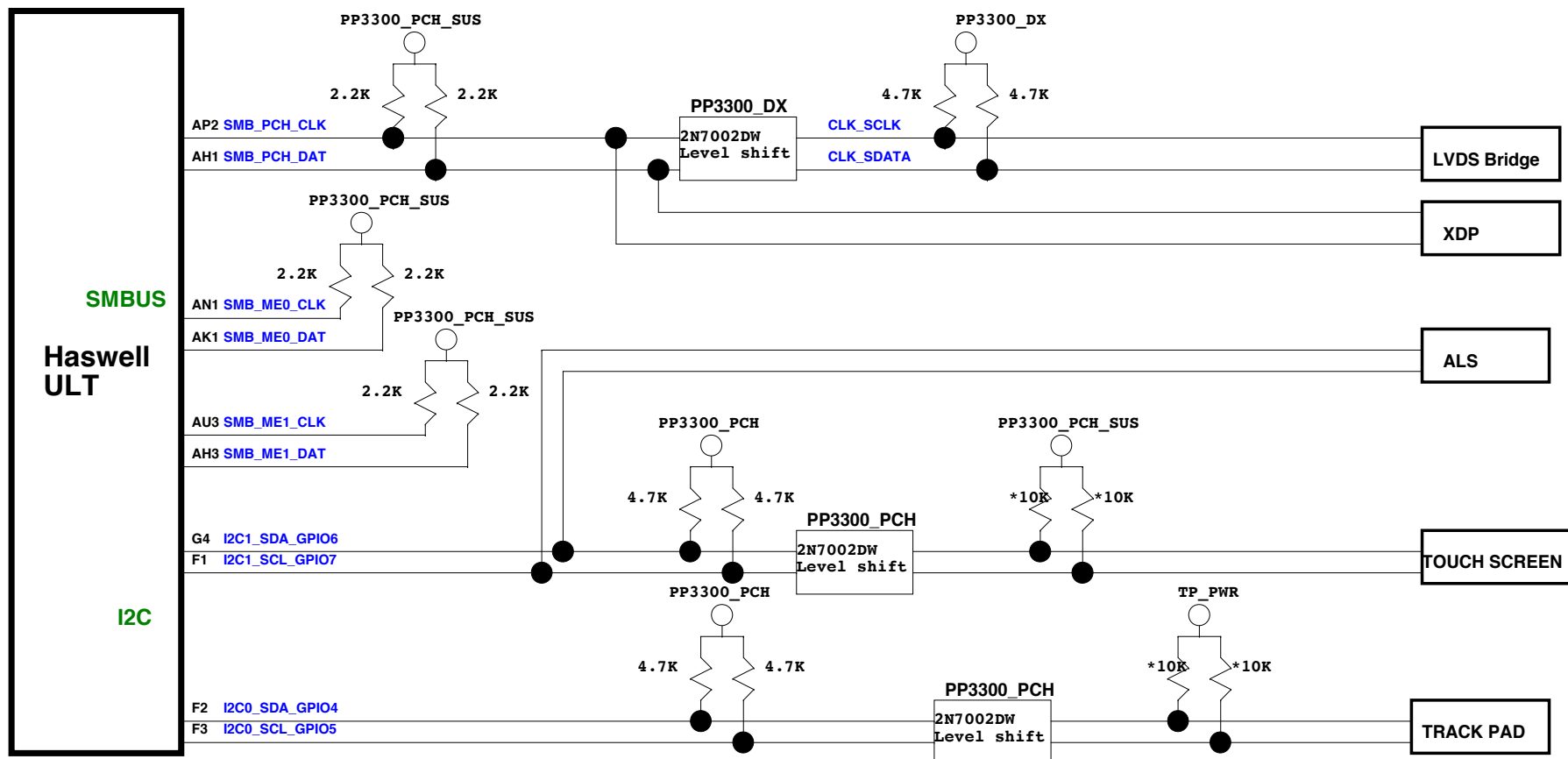
[10,19,25] PP3300\_WLAN\_EN  PP3300\_WLAN\_EN PR168 \*Short\_4 PP3300\_WLAN\_EN\_R

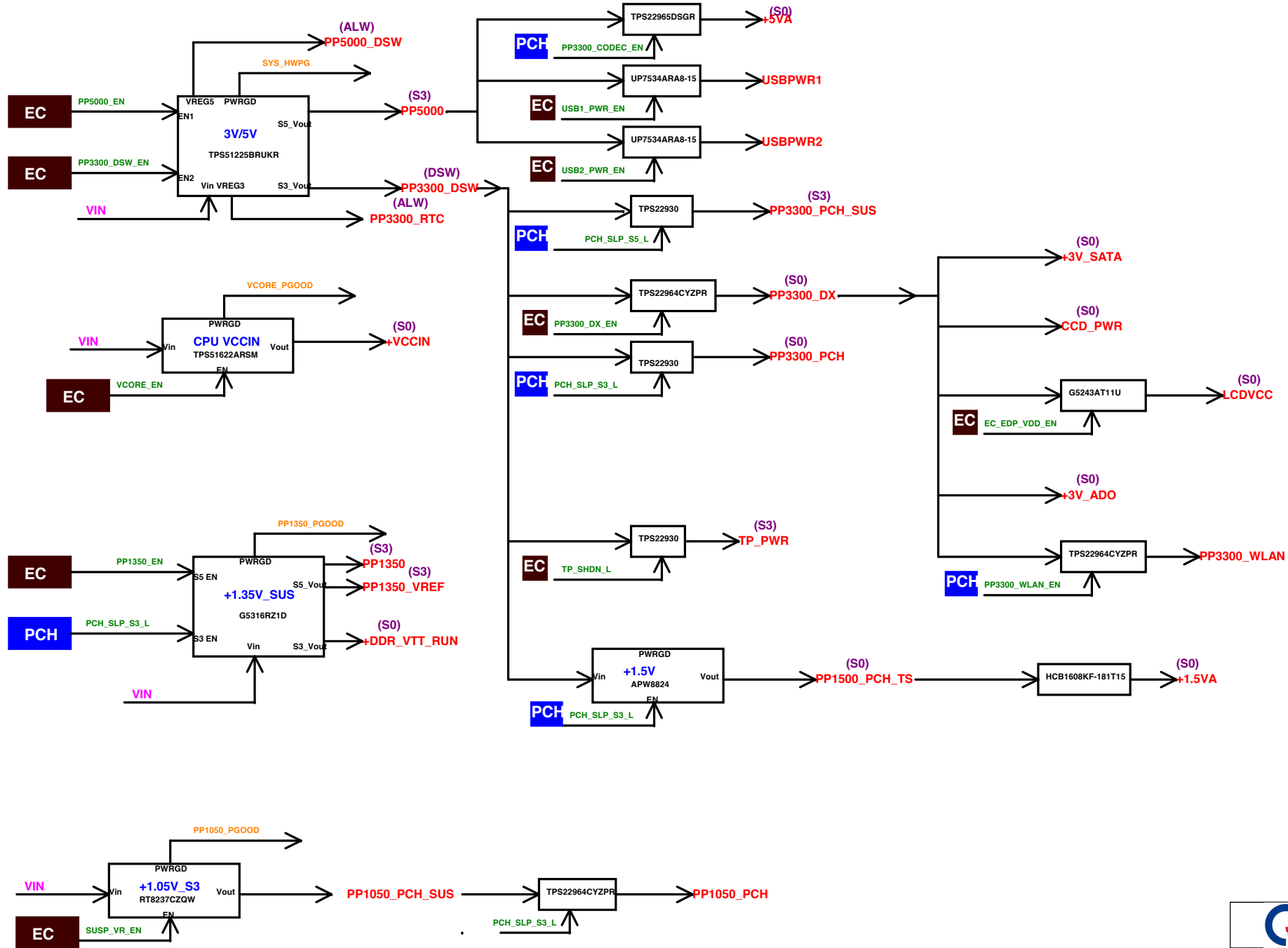


[7,25] PCH\_SLP\_SUS\_L  R115 \*Short\_4 PCH\_SLP\_S5\_L\_R

[7,13,25,29] PCH\_SLP\_S5\_L  PCH\_SLP\_S5\_L R112 \*0.4







[illegible]